Solar Array Emulator

by

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Date: ....December 2016

Abstract

Solar Array Emulator

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A typical photovoltaic (PV) system normally consists of the following elements: PV energy generator (cell, module or array), PV power electronic systems (grid-tie inverter or maximum power point tracker (MPPT) or battery charge controller) and the load (energy consumer). The efficiency in power transfer from the source to the load, largely depends on the impact of the environmental conditions on the PV module's performance and the electrical characteristics of the PV power electronic systems. Varying environmental conditions causes the non-linear output characteristics of the PV modules to change. In addition, the PV power electronics systems must be well suited to adapt to the change of the PV module's output characteristics in order to ensure power transfer at highest efficiency. Different control strategies have been developed that controls the electrical characteristics of these systems to ensure maximum available power is delivered to the load.

The manufactures and laboratories dedicated to the design and development of the PV power electronic systems, are faced with a responsibility of evaluating, optimising and certifying these systems according to specific performance standards. The conventional approach used to evaluate these systems involves having to conduct outdoor field experiments. The processes in field experiments involve having to connect actual PV modules to these systems. Moreover, the performance evaluation process is based on the power yield of the systems under the present environmental conditions. However, the processes are limited to the present environmental conditions albeit thorough evaluations under many different operating conditions are necessary. Therefore the conventional approach

is largely dependent on environmental conditions. Furthermore, the approach is costly, time consuming and requires a lot of resources.

In this thesis, a more appropriate and flexible approach is proposed. A system called the Solar Array Emulator (SAE) is designed and developed that is responsible for the performance evaluation of the PV power electronic systems. The SAE is a controllable indoor test facility that emulates the static and dynamic non-linear output characteristics of an actual PV module or array. A graphical user interface (GUI) is designed that allows the user to define the operating environmental conditions and the parameters of the actual module or array to be emulated. Based on the user-defined specifications, the SAE emulates the non linear output characteristics of an actual module. In addition, the SAE facilitates the evaluation of the PV power electronic systems' performance in steady-state and dynamic-state under different load and environmental conditions. The SAE has the advantage of being user friendly, flexible, compact and ensures thorough evaluation processes.

The practical experiments conducted indicate that the proposed SAE system is able to successful emulate the dynamic and static characteristics of an PV module or array under different environment conditions. The experimental performance evaluations of two PV power electronics systems namely the grid-tie inverter and the maximum power point tracker are conducted using SAE. The experimental results obtained verifies the suitability of the proposed SAE to facilitate the performance evaluation of PV power electronic systems.

Uittreksel

Sonkrag Array Emulator

("Solar Array Emulator")

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'n Tipiese foto-voltaïese stelsel bestaan gewoonlik uit die volgende elemente: foto-voltaïese energie kragopwekker (sel, module of skikking), foto-voltaïese drywingselektronika stelsels (netwerk gekoppelde omsetter of maksimum kragpunt volger of battery beheerder) en die las (energie verbruiker). Die doeltreffendheid van die stelsel hang grootliks vanaf die impak van die omgewings kondisies op die foto-voltaïese module en die elektriese eienskappe van die foto-voltaïese drywingselektronika stelsels. Wisselende omgewingstoestande veroorsaak dat die nie-lineêre uittree kenmerke van die PV modules verander. Daarbenewens moet die foto-voltaïese drywingselektronika stelsels geskik wees om aan te pas by die verandering van die uittree kenmerke van die foto-voltaïese module, om drywingsoordrag by hoogste doeltreffendheid te verseker. Verskillende beheer strategieë is al ontwikkel wat die elektriese eienskappe van hierdie stelsels beheer om te verseker maksimum beskikbare krag is aan die las gelewer.

Die vervaardig en laboratoriums opgedra aan die ontwerp en ontwikkeling van die foto-voltaïese drywingselektronika stelsels is te make met 'n verantwoordelikheid van die evaluering, die optimalisering en sertifiseer hierdie stelsels volgens spesifieke prestasiestandaarde. Die konvensionele benadering wat gebruik word om hierdie stelsels te evalueer behels om buite in die veld eksperimente uit te voer. Die prosesse in veldeksperimente behels dat die werklike foto-voltaïese modules aan sluit op hierdie stelsels. Daarbenewens is die prestasie-evaluering proses wat gebaseer is op die krag opbrengs van die stelsels onder

die huidige omgewingstoestande. Tog is die prosesse beperk tot die huidige omgewingstoestande, hoewel deeglike evaluering onder baie verskillende bedryfstoestande nodig is. Daarom is die konvensionele benadering grootliks afhanklik van omgewingstoestande. Verder is die benadering tydrowend en vereis baie hulpbronne en is duur.

In hierdie tesis, is 'n meer gepaste en buigsame benadering voorgestel. 'n Stelsel genoem "Solar Array Emulator"(SAE) is ontwerp en ontwikkel, wat verantwoordelik is vir die prestasie-evaluering van die PV drywingselektronika stelsel. Die SAE is 'n beheerbare binnemuurs toetsfasiliteit wat die statiese en dinamiese nie-lineêre uittree kenmerke van 'n werklike PV module of skikking naboots. 'n Grafiese gebruikerskoppelvlak is ontwerp wat die gebruiker toelaat om die bedryf omgewingstoestande en die parameters van die werklike module of skikking wat nagevolg word, te definieer. Gebaseer op die gebruiker-gedefinieerde spesifikasies, die SAE naboots die nie-lineêre uittree kenmerke van 'n werklike module. Daarbenewens vergemaklik die SAE die evaluering van die prestasie van die foto-voltaïese drywingslektronieka stelsel in gestadige en dinamiese toestand onder verskillende las en omgewingstoestande. Die SAE het die voordeel dat dit gebruikersvriendelik, buigsame, kompak en verseker deeglike evaluering prosesse.

Die praktiese eksperimente dui daarop dat die voorgestelde SAE stelsel in staat is om suksesvol die dinamiese en statiese eienskappe van 'n PV module of skikking onder verskillende omgewing voorwaardes te naboots. Die eksperimentele prestasie evaluerings van twee PV drywingselektronika stelsels, naamlik die netwerk gekoppelde omsetter en die maksimum kragpunt volger, is uitgevoer met behulp van SAE. Die eksperimentele resultate bevestig die geskiktheid van die voorgestelde SAE om die prestasie-evaluering van PV krag elektroniese stelsels te fasiliteer.

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- Professor Mouton for his endless support and greatest humour.
- Dr Rix for his insights and support.
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- My family for their prayers and love.
- Wendy for her encouragements.
- Arimand and Dr Strauss for assisting in carrying out experiments.
- Scatec Solar company for its financial support.

Dedications

To the champion, Delvin

List of Publications

- **SAUPEC 2015**
  Inner Loop Current Controller Design for a Solar Array Emulator
  In this paper the design and modelling of a PI Current Controller and Pulse Width Modulator (PWM) implemented on Field Programmable Gate Arrays (FPGA) for a Solar Array Eimulator (SAE) system are described. The SAE system should accurately emulate the I-V curve characteristics of different arrays under various environmental conditions i.e temperature, irradiation and shading. This entails that the controller should be fast and accurate and the SAE system should remain stable under different kinds of load systems. The analysis of the continuous signal control processes closely approximates highly over-sampled digital current controllers. The small-signal model of the Pulse Width Modulator (PWM), illustrates how the duty cycle behaves with small perturbations in reference current. A small-signal model based method is derived and presented that enables the design of a stable controller.

- **SASEC 2016**
  Solar Array Emulator
  In this paper is a description of the design and development of a system responsible for performance evaluation of photovoltaic energy production systems such as DC/AC and grid-tie inverters, maximum power point trackers, etc. is presented. The system developed is called a Solar Array Emulator (SAE). The system is composed of a DC/DC synchronous buck converter, graphical user interface (GUI) running on personal computer (PC), and an FPGA device. The FPGA device runs the current feedback control architecture of the SAE system and controls the switching behaviour of the DC/DC converter based on the pulse width modulation (PWM) principle. The system, using the GUI allows the user to define PV array parameters, weather conditions and the degree of partial shading. The SAE system rated at 20 kW is tested using a variable resistor and a grid-tie inverter. The experimental results indicate that the proposed SAE system emulates the current-voltage (I-V) profile of an actual array with an average percentage deviation of 1.5%.

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Nomenclature

Constants

c	=	$3.8 \times 10^{8}\,\mathrm{m\,s^{-1}}$
h	=	$6.626 \times 10^{-34}\,\mathrm{J\,s}$
k	=	$1.381 \times 10^{-23}\,\mathrm{J\,K}$
q	=	$1.602 \times 10^{-19}\,\mathrm{C}$

Variables

f_s	Switching frequency
I_{mp}	Current at maximum power point
I_{SC}	Short circuit current
K_I	Integral gain
K_P	Proportional gain
K_{SS}	Small-signal gain
P_{max}	Power at maximum power point
$\dot{r_o}$	Ripple gradient
T_s	Switching period
V_{mp}	Voltage at maximum power point
V_{OC}	Open circuit voltage

Abbreviations

A/D	Analog to Digital
AC	Alternating current
CS	Chip Select
DC	Direct Current
DSP	Digital Signal Processing
FF	Fill Factor

FPGA	Field Programmable Gate Array
GUI	Graphical User Interface
IGBT	Insulated Gate Bipolar Transistor
IC	Integrated Circuit
I-V	Current-Voltage
LUT	Look Up Table
LSB	Least Significant Bit
MPPT	Maximum Power Point Tracking
MSB	Most Significant Bit
NOCT	Nominal Operating Cell Temperature
P&O	Perturb and Observe
P-V	Power-Voltage
PC	Personal Computer
PCB	Printed Circuit Board
PI	Proportional Integral
PV	Photovoltaic
PWM	Pulse Width modulation
RMS	Root Mean Square
SCLK	Serial Clock
SPI	Serial Peripheral Interface
SVPWM	Space Vector Pulse width modulation
UART	Universal Asynchronous Receiver/Transmitter
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit

Chapter 1

Introduction

Over the years, there has been a growing interest in the sustainable and environmentally friendly means of generating electricity as a supplement to or replacement for the already existing means of generating electricity. The escalating global demand for energy is among the leading reasons behind the quest for a sustainable means of generating electricity by using renewable energy resources. The renewable energy resources, particularly solar photovoltaic (PV) energy, are perceived as good alternatives. On the other hand, the existing means of generating electricity, by utilising non-renewable energy resources such as oil, natural gas, coal and uranium are hazardous to the environment. Harnessing these non-renewable energy resources is associated with the production of by-products such as photochemical pollutants and green house gases that cause air pollution and the depletion of the ozone layer resulting in global warming.

Such effects on the environment associated with the harnessing of non-renewable energy resources, are also the leading reasons intensifying interest in renewable energy. The processes for harnessing renewable energy resources produces hardly any waste products such as photochemical pollutants or green house gasses that threaten the environment. Therefore renewable energy is a clean source of energy that offers a solution to sustainable development, carbon footprint management and energy security.

1.1 Solar photovoltaic energy

Solar PV energy is widely favoured as it is naturally replenished and is available in abundance in most parts of the world at no cost. Moreover, the sun, which is the source of energy, is capable of supplying solar energy indefinitely. Solar power generation has consequently reduced the increased dependence on fossil fuels such as oil, coal, gas, etc. for meeting the energy demand. Furthermore, cutting over-reliance on fossil fuels has also reduced the cost involved in importing and transporting the fossil fuels and therefore

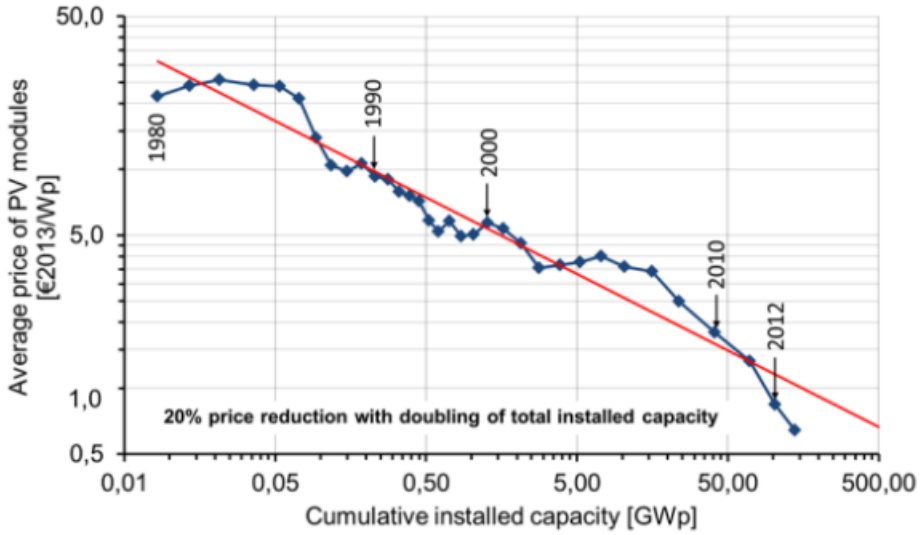

Figure 1.1: Historical change in solar module pricing. The red line indicates the pricing trend [1]

the saved financial resources are channeled towards investments in renewable energy . Moreover, the systems responsible for harnessing solar energy are durable and generally requires minimum maintenance when compared to systems responsible for harnessing energy from fossil fuels. For such reasons aforementioned, among others, many projects across the world have been initiated for solar power generation for grid supply or off-grid small to medium-sized applications in remote communities.

Since the advent of solar PV modules, there has been a considerable decrease in their pricing over the years. The downhill trend in the price of solar modules over a couple of years is illustrated in Figure 1.1. Moreover, due to the improvements in the technological design of solar PV modules in recent years, their efficiency has increased considerably. An uphill trend in the efficiency of solar PV modules over the years is shown in Figure 1.2. As a result of improved efficiency and affordability, solar energy has become a worthwhile investment and a remarkable increase in installation capacity is observed across the world.

1.2 Thesis motivation

A typical PV system normally consists of the following elements: PV energy generator (cell, module or array), PV power electronic systems (grid-tie inverter or maximum power point tracker (MPPT) or battery charge controller) and the load (energy consumer). The overall performance of the solar PV systems is the summation of the efficiencies of all the elements involved from the source to the load. These elements must operate at their maximum efficiency in order to deliver maximum power to the load.

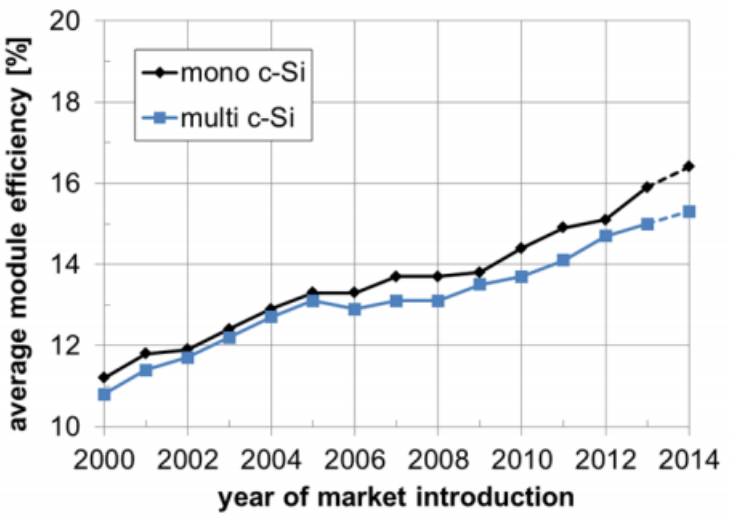

Figure 1.2: Growth in mean efficiency of PV modules, based on mono- and multicrystalline solar cells [1]

A PV module has non-linear output characteristics influenced by the module's parameters e.g. open circuit voltage V_{oc} and short circuit current I_{sc}. Moreover the module's non-linear output characteristics are influenced by the operating environmental conditions such as temperature, solar irradiation, wind speed, altitude and partial shading. Figure 1.3 shows the non-linear current-voltage (I-V) and power-voltage (P-V) characteristic curve of a PV module with I_{sc} of 2 A and V_{oc} of 20 V operating at temperature of 25 °C and irradiation of 1000 W m^{-2}. Moreover, Figure 1.4 shows the non-linear I-V and P-V characteristic curve of a one-cell shaded module with the same parameters and operating conditions. In both figures, V_{mp} and I_{mp} indicates the voltage and the current at the operating point P_{max} that will yield maximum power.

In order for the PV power electronic systems connected to the solar module to operate at their maximum efficiency, they should be able to adapt to the rapidly changing output characteristics of a solar PV module shown in Figure 1.3 and Figure 1.4. Therefore these systems should be evaluated and certified according to specific performance standards prior to commercialisation and installation on site. This will ensure that the power electronic systems will be optimised for maximum operating efficiency before installation. The conventional approach of evaluating the PV power electronic systems prior to installation is an outdoor field-testing process. However such an approach has major drawbacks as the process is tedious, costly, dependent on weather conditions and also time consuming. Furthermore, an outdoor field test would require real solar panels. In addition, tests are limited to the actual weather conditions, although tests under certain but non-achievable conditions (e.g. extra-terrestrial solar irradiation, cold temperature in hot climate conditions and vice versa) would be fundamental in a thorough evaluation

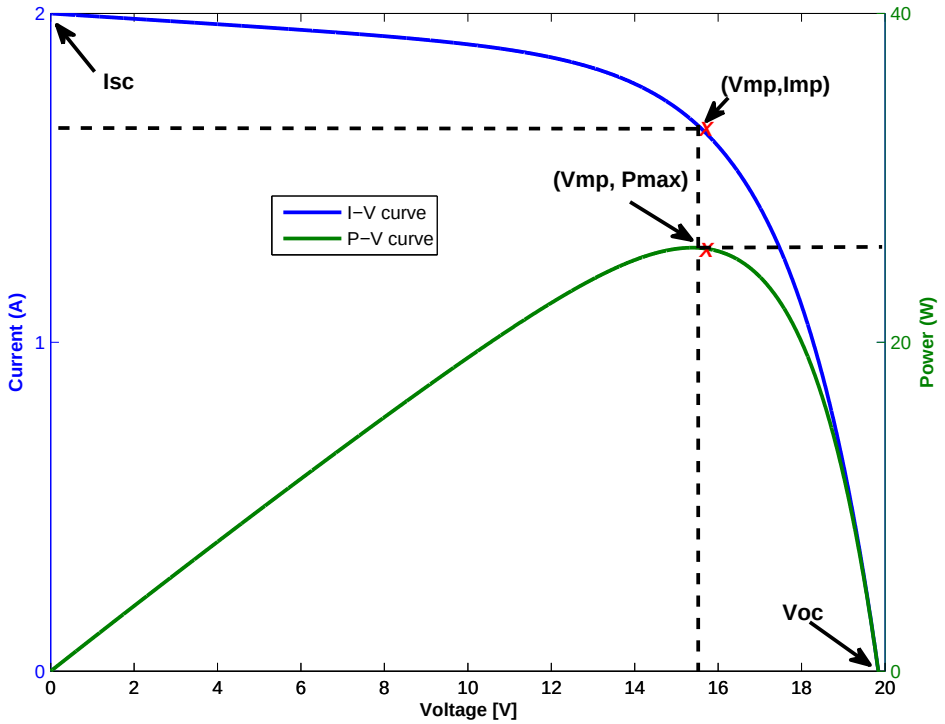

Figure 1.3: I-V and P-V characteristic curve of a photovoltaic module

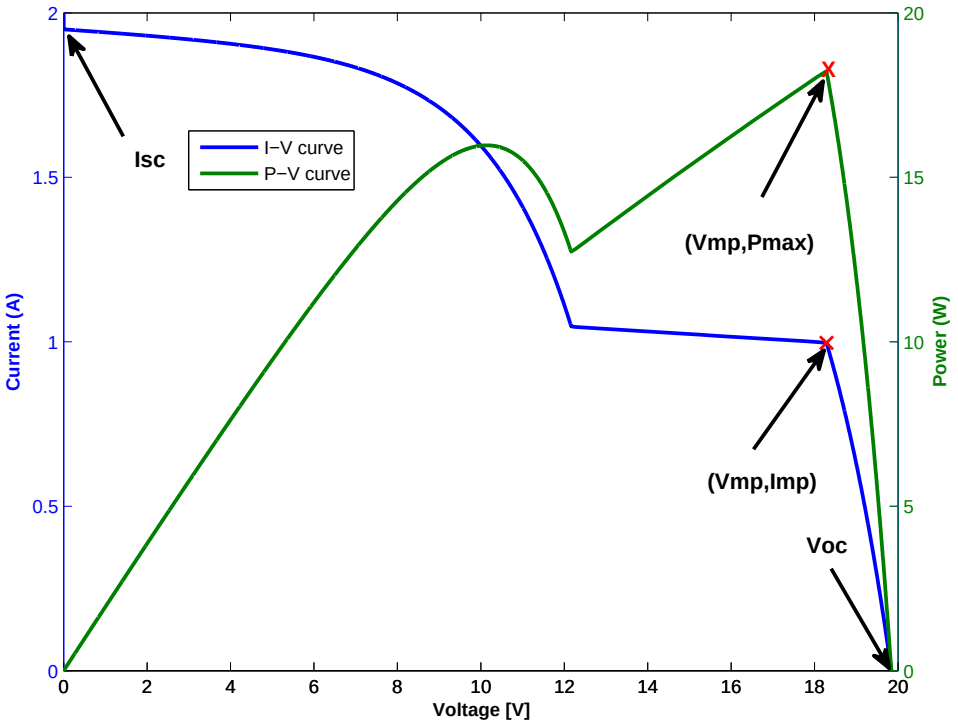

Figure 1.4: I-V and P-V characteristic curve of a one-cell shaded photovoltaic module

process.

1.3 Thesis objectives

This research proposes an alternative to the conventional approach of evaluating the performance of the PV power electronic systems. This project entails the design and development of a standalone system that facilitates the evaluation process of the PV power electronic systems such as inverters, battery charge controllers and maximum power point trackers. The proposed system is called the Solar Array Emulator (SAE). The purpose of the SAE is to provide a controllable indoor-test facility that can emulate the non-linear current-voltage output characteristics of an actual PV module or array. The detailed overview of the SAE system is given in Chapter 3 and its hardware and control strategy designs are discussed in greater detail in Chapter 4 and Chapter 5, respectively. The SAE is able to emulate the I-V output characteristics of a PV module or array under different temperature, solar irradiation and partial shading conditions. Therefore, the SAE is able to facilitate the performance evaluation of the PV power electronics systems at normal and extreme conditions. The developed SAE has the advantages of conducting a thorough evaluation process, being user friendly and cost effective.

1.4 Thesis Outline

This thesis consists of 8 chapters and below is a brief description of what is included in each chapter.

In **Chapter 2** the literature about developed models that ideally characterise the behaviour of PV cells is analysed. The principle of operation of solar cells based on the different models is discussed in order to help understand how the effects of temperature, irradiation and partial shading influence the overall performance and efficiency of a PV module. Mitigation strategies against the effects of shading are also discussed. Published articles on existing designs of solar array emulators are also discussed including their design methodologies.

In **Chapter 3** how the developed SAE operates is described. The technique employed by the SAE in emulating the behaviour of an actual PV module is discussed. Furthermore, the functions of the FPGA board in transmitting gate signals, sensing current and voltage, serial communication and running current control algorithm are described. Moreover, the developed algorithms responsible for UART serial communication, the pulse-width modulation principle, analog to digital conversion and the dead time are discussed through the use of finite state machines.

In **Chapter 4** the design and operation of the DC/DC synchronous buck converter is discussed. The in-depth design strategies employed in designing the filter capacitor, bus capacitor and the inductor, based on the converter specifications are discussed. In addition, the design and construction of the voltage and current sensors is described. Power losses occurring in the converter are calculated in order to determine the heat sink specifications. Furthermore, the design and operation of the auxiliary circuits such as isolated power supply and gate driver circuitry are described.

In **Chapter 5** the controller design strategies for a single loop current controller and a dual loop voltage controller are discussed. The classical strategy of implementing an average model is designed and tested in simulation. Another approach called the small-signal model is implemented in designing the single and dual closed loop controllers. A comparison is carried out between the two design models in order to determine the best model that can accurately predict stability margins of both the single and the dual loop controllers.

In **Chapter 6** the simulation results of the SAE operating in simulation mode are discussed. A graphical user interface (GUI) is presented that enables the user to simulate the I-V and the P-V characteristic curves of a PV module or array. The I-V and P-V characteristic curves for different conditions are analysed and discussed.

In **Chapter 7** emulation mode experimental results are presented. The SAE emulates the I-V characteristic curves of different array configurations operating under different environmental conditions. The SAE is tested for steady state and dynamic response using the variable resistor. Furthermore, the SAE is used to evaluate the performance of the grid-tie inverter and an MPPT active load under different operating conditions.

In **Chapter 8** an overview of the project's conclusions and recommendations on how the system can be further improved are given.

Chapter 2

Literature Review

The fundamental theoretical concepts relevant to the design of the Solar Array Emulator (SAE) system are analysed in this chapter.

In order to comprehend the physics involved in converting sunlight to electricity, the starting point is to analyse the elementary component in photovoltaic systems which is the photovoltaic cell. Photovoltaic (PV) cells convert the energy contained in photons of sunlight into an electrical voltage and current. These cells are made from semiconductor materials i.e Group IV and Group V elements. In the past, silicon, a Group IV element, which comprises approximately 20% of the earth's crust, dominated in PV industry in the manufacture of PV cells. However, there is emerging competition from more efficient compound materials formed by pairing elements in different groups e.g. gallium arsenide (GaAs) formed by pairing gallium a Group III element and arsenide a Group V element.

2.1 A generic PV cell

The principle of operation of a PV cell is illustrated in Figure 2.1 . A PV cell is formed when two oppositely doped semiconductor materials namely the p-type and the n-type materials are connected to each other to form a p-n junction. Doping is a chemical process during which impurities are added to semiconductor materials in order to alter their properties. The most important factor that doping affects is the material's charge concentration i.e it results in the material containing either a surplus of positive charge carriers (p-type material) or a surplus of negative charge carriers (n-type material). Therefore the p-type material has an excess of holes and the n-type material has an excess of electrons.

Generally semiconductor materials are perfect electrical insulators at absolute zero temperature as charge carriers (electrons) are immobile due to the electrostatic force of attraction imposed by the nucleus [2]. Electrons in an atom can only exist in allowable energy bands and the gaps between them are called forbidden bands. The furthest band

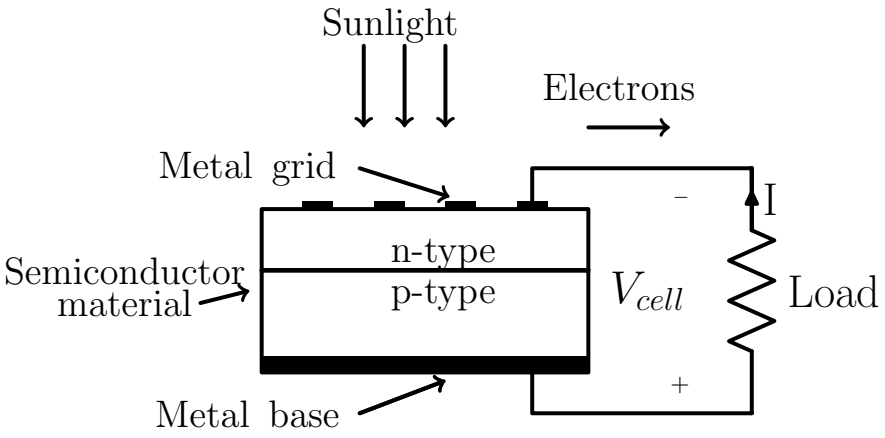

Figure 2.1: Physical structure of PV cell

from the nucleus is the conduction band and if an electron exists in this band, it is free to roam around in the crystal. In order for an electron to jump across the forbidden bands into the conduction band, the electron must acquire energy called band-gap energy E_g. In photovoltaics, the energy equivalent to the bang-gap energy is acquired from photons of the electromagnetic energy from the sun. The energy of the photon is based on Equation 2.1.1 where h is Planck's constant ($6.626 \times 10^{-34}\,\mathrm{J\,s}$), c is the speed of light ($3 \times 10^{8}\,\mathrm{m\,s^{-1}}$) and λ is the wavelength (m) of the photon.

$$E = \frac{hc}{\lambda} \tag{2.1.1}$$

According to Figure 2.1, the electrical contacts are attached to the top of the n-type material and to the bottom of the p-type material. A p-n junction exists where both the p-type and n-type materials are connected together. When the vicinity of the p-n junction is exposed to sunlight, photons with energy equal to the band-energy are adsorbed by the PV cell, creating hole-electron pairs. Electrons will flow out of the n-type material into the connecting wire, through the load and back to the p-type material, as shown in Figure 2.1. Since holes cannot be conducted, it is only electrons that flow around the circuit. When the electrons reach the p-type material, they recombine with holes and thereby completing the circuit. By convention, current flows in the direction opposite to the electron flow. Therefore a current will continue to flow as long as the PV cell is exposed to sunlight and receiving photons with sufficient energy.

In order to help predict the performance of PV cells, engineers designed several models that ideally characterise their behaviour. In the following sections, the different models of PV cells are analysed. Moreover the effects of shading, temperature and irradiation are discussed later in the chapter.

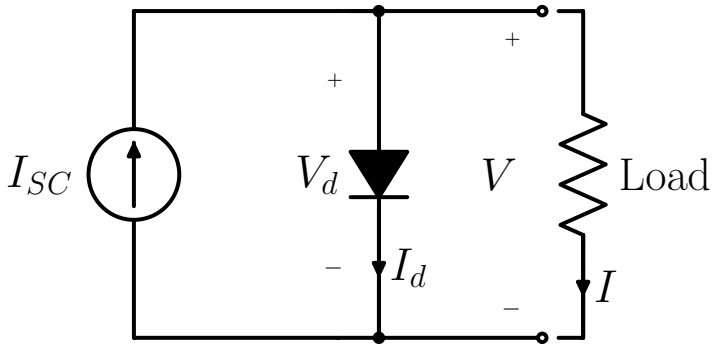

Figure 2.2: PV cell simple equivalent circuit

2.2 Equivalent circuits of a solar cell

The different equivalent models vary in terms of accuracy and complexity and are made of discrete idealised electrical components with well defined properties. In this section, a simple model of a solar cell shown in Figure 2.2 and a more sophisticated model shown in Figure 2.3, are discussed.

2.2.1 Simplest equivalent circuit

The model in Figure 2.2, is made up of an ideal current source in parallel with a real diode. The current source delivers current in proportion with the solar irradiation incident on the cell. There are two most crucial parameters in photovoltaic systems namely the short circuit current I_{sc} and the open circuit voltage V_{oc}. When the leads of the PV cell equivalent model in Figure 2.2 are shorted, current no longer flows through the diode i.e. $V_d = 0$ and all the current flows through the shorted leads.

Therefore the magnitude of I_{sc} becomes equal to the current flowing from the ideal current source. However when the load is connected as shown in Figure 2.2, the current flowing through the load is described by Equation 2.2.1 where I_d is the current through the diode.

$$I = I_{sc} - I_d \tag{2.2.1}$$

Moreover, the current-voltage (I-V) characteristics curve for the p-n junction diode is described by the Shockley diode equation in Equation 2.2.2 where k is Boltzmann constant valued at $1.381 \times 10^{-23}\,\mathrm{J\,K^{-1}}$, T is the junction temperature measured in Kelvins (K), q

is the electron charge valued at 1.602×10^{-19} C and V_d is the voltage across the diode.

$$I_d = I_o \left(e^{\frac{qV_d}{kT}} - 1 \right) \tag{2.2.2}$$

The term I_o denotes the reverse saturation current of the diode. The reverse saturation current I_o is directly related to the recombination of electrons and holes but inversely related to the material quality. Substituting Equation 2.2.2 into Equation 2.2.1 gives Equation 2.2.3 which describes the amount of current through the load.

$$I = I_{sc} - I_o \left(e^{\frac{qV_d}{kT}} - 1 \right) \tag{2.2.3}$$

When the leads of the solar cell equivalent model are left open i.e. $I = 0$, the open circuit voltage V_{oc} is obtained by re-arranging Equation 2.2.3 and solving for V_d. The resulting V_d is equivalent to V_{oc} and is given by Equation 2.2.4.

$$V_{oc} = \frac{kT}{q} \ln \left(\frac{I_{sc}}{I_o} + 1 \right) \tag{2.2.4}$$

2.2.2 A more accurate solar cell equivalent circuit

The simple equivalent model described previously, poses some limitations in the event of cell shading by a tree, building etc. For instance if two series-connected cells are connected to a load, the simple model suggests that virtually no current flows to the load if one of the cells is completely shaded. The diode of the shaded cell would be reverse biased and therefore it does not allow any current through except for the tiny amount of reverse saturation current. Therefore such a simple model is applicable only where high modelling accuracy is not desired.

However, in order to overcome the shortcomings of the simple model, a more sophisticated model is employed. Figure 2.3 shows a more complex equivalent circuit of a PV cell that incorporates series resistance R_s and parallel leakage resistance R_p. In Figure 2.3, the amount of current flowing through the load is described by Equation 2.2.5 where I_p is the current through the parallel leakage resistance and equivalent to $\frac{V_d}{R_p}$.

$$I = I_{sc} - I_d - I_p \tag{2.2.5}$$

The voltage across the diode V_d is given by Equation 2.2.6.

$$V_d = V + IR_s \tag{2.2.6}$$

This means that the voltage across an individual cell is given by Equation 2.2.7.

$$V = V_d - IR_s \tag{2.2.7}$$

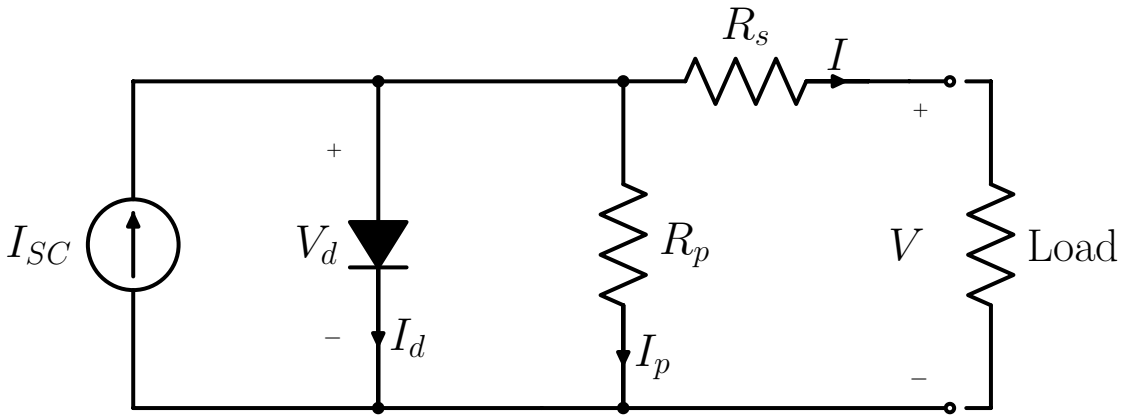

Figure 2.3: A more complex PV cell equivalent circuit

Therefore the current-voltage relationship of the sophisticated model is given by Equation 2.2.8.

$$I = I_{sc} - I_o \left(e^{\frac{q}{kT}(V+IR_s)} - 1 \right) - \left(\frac{V + IR_s}{R_p} \right) \tag{2.2.8}$$

Unfortunately, Equation 2.2.8 is a complex equation that does not have an explicit solution for either V or I. However a spreadsheet solution is suggested that has the advantage of representing the relationship between I and V according to Equation 2.2.8 in the form of a curve. The I-V curve representation of a string of cells is discussed in Section 2.2.4.

2.2.3 PV Cells to Modules to Arrays

An individual cell produces about 0.5 V which is not sufficient enough to drive a number of applications [2]. Therefore the basic building block for PV applications is a module which consists of a number of cells wired in series. When the cells are wired in series in a module, all the cells carry the same current and the voltage across the module is found by multiplying the voltage across an individual cell shown in Equation 2.2.7 by the number of cells n in the module as shown in Equation 2.2.9.

$$V_{module} = n(V_d - IR_s) \tag{2.2.9}$$

Multiple modules can be wired in series to increase voltage and in parallel to increase current. This in turn will increase the power generated. The combination of modules in series and in parallel gives rise to an array.

2.2.4 I-V characterstic curve

The current-voltage I-V characteristic curve of a module is derived primarily from the complex equation shown in Equation 2.2.8. The current and the voltage of a module

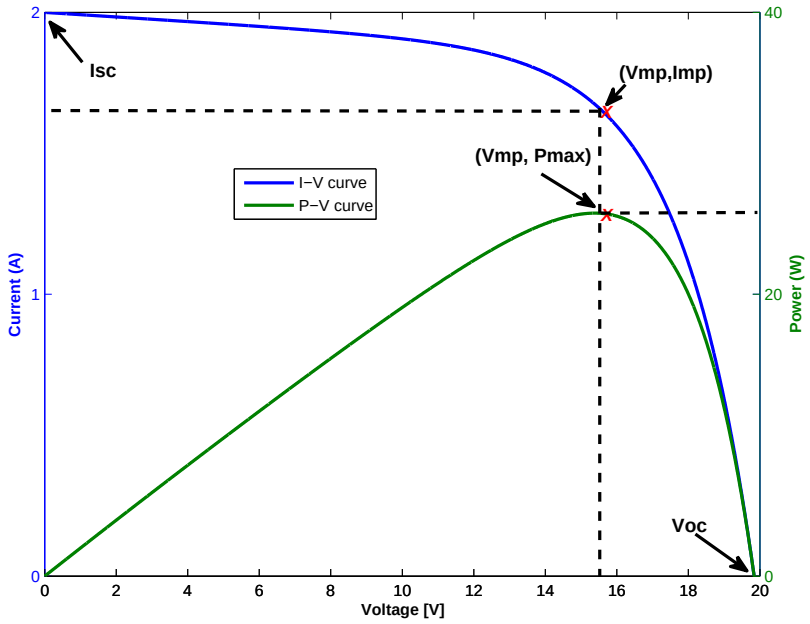

Figure 2.4: I-V and P-V characteristic curve of a PV module operating at a temperature of 25 °C and an irradiation of 1000 W m^{-2}

varies depending on the operating environmental conditions e.g degree of shading, the ambient temperature and irradiation levels. The effects of these conditions are discussed later in the chapter. Figure 2.4 shows the non-linear I-V and the power-voltage (PV) characteristic curves of a module simulated, based on Equation 2.2.8. The I-V and P-V characteristic curves are simulated at standard test conditions i.e. at a cell temperature of 25 °C and an irradiation of 1000 W m^{-2}. The module has a short circuit current I_{sc} of 2 A and a open circuit voltage V_{oc} of 20 V.

For a specific optimum load, the simulated module will operate at the maximum power point labelled (V_{mp}, P_{max}). The current and voltage at maximum power point are I_{mp} and V_{mp}, respectively as shown in Figure 2.4. A parameter known as the fill factor FF is used to characterise the module performance i.e the FF is used to determine the quality of a particular module. The fill factor is the ratio of the power at the maximum power point to the product of V_{oc} and I_{sc}. Therefore FF is described by Equation 2.2.10.

$$FF = \frac{V_{mp}I_{mp}}{V_{oc}I_{sc}} \tag{2.2.10}$$

2.3 Environmental factors affecting photovoltaic systems' performance

Several factors affect the overall performance of a module or an array of modules. These environmental factors include shading, ambient temperature and irradiation levels. These conditions are non-controllable and photovoltaic systems are designed to adapt to such ever-changing conditions. Below are some of the insights pertaining to the effects of shading, temperature and irradiation on the performance of photovoltaic systems.

2.3.1 Effects of Temperature and Radiation

Manufactures of photovoltaic systems will often provide the I-V characteristic curves illustrating the behaviour of photovoltaic modules with varying irradiation. Changes in irradiation evoke a change in short circuit current I_{sc} in direct proportion and a modest reduction in open circuit voltage V_{oc} [3]. For example dropping the irradiation levels by half, drops the short circuit current I_{sc} by half also and this decreases the power output. Moreover, if the cell temperature increases, the open circuit voltage V_{oc} drops by a considerable amount and the short circuit current slightly increases [2, 4]. The operating cell temperature is determined by the equilibrium between the ambient operating temperature, the heat generated by the module and the heat lost to the environment by the module.

Considering the significant shift in cell performance due to temperature changes, manufactures provide an indicator called nominal operating cell temperature (NOCT). This indicator helps account for changes in cell performance due to temperature changes. NOCT is defined as the expected cell temperature T_{cell} in a module when ambient temperature T_{amb} is 20 °C, solar irradiation G is 800 W m^{-2} and wind speed is 1 m s^{-1} [5]. To account for the cell temperature at other ambient conditions, Equation 2.3.1 is used.

$$T_{cell} = T_{amb} + \left(\frac{NOCT - 20}{800}\right) G \tag{2.3.1}$$

The current through the diode I_d in Equation 2.2.2, is affected by the change in operating temperature conditions T_{cell}. The reverse saturation current I_o in Equation 2.2.2 is measured at standard conditions and as the cell temperature changes, the reverse saturation current also changes according to Equation 2.3.2 [6]. $I_{o,T_{STC}}$ denotes the reverse saturation current at standard testing conditions (STC) and $I_{o,Tcell}$ denotes the reverse saturation current at cell temperature T_{cell}. Moreover Eg is the band gap energy and a

is the quality factor of the diode.

$$I_{o,Tcell} = I_{o,T_{STC}} \left(\frac{T_{cell}}{T_{STC}}\right)^3 e^{[\frac{qEg}{ak}(\frac{1}{T_{cell}} - \frac{1}{T_{STC}})]} \tag{2.3.2}$$

The dependence of the short circuit current $I_{sc,T_{cell}}$ and the open circuit voltage $V_{oc,T_{cell}}$ on changes in temperature and solar irradiation are described by Equation 2.3.3 and Equation 2.3.4 respectively. These equations are used in [2].

$$I_{sc,Tcell} = \frac{G}{G_{STC}}(I_{sc,STC} + \mu_{I,sc}(T_{cell} - T_{STC})) \tag{2.3.3}$$

$$V_{oc,Tcell} = V_{oc,STC}(1 + \mu_{V,oc}(T_{cell} - T_{STC})) \tag{2.3.4}$$

Where $\mu_{I,sc}$ and $\mu_{V,oc}$ are the thermal drifts of I_{sc} and V_{oc}, respectively. $V_{oc,STC}$ is the open circuit voltage and $I_{sc,STC}$ is the short circuit current of the module measured at standard test conditions i.e G_{STC} of $1000\,\mathrm{W\,m^{-2}}$ and T_{STC} of $25\,^{\circ}\mathrm{C}$. The current I that flows through the load at T_{cell} is described by Equation 2.3.5.

$$I = I_{sc,Tcell} - I_{o,Tcell}\left(e^{\frac{q}{kT_{cell}}(V+IR_s)} - 1\right) - \left(\frac{V + IR_s}{R_p}\right) \tag{2.3.5}$$

2.3.2 Effect of shading

Photovoltaic modules are very sensitive even to small amounts of shading. When a module is one-cell shaded, the power output of the entire module can be significantly reduced [7]. Moreover, the performance of a string of modules can be affected if a single module in the string is shaded. Shading in a module is caused by a number of factors e.g. dust accumulation, bird droppings, shading by tall buildings or trees, etc. In order to understand the phenomenon of shading, the physics of shading is discussed below. Mitigation measures to curb the effects of shading are also discussed.

2.3.2.1 Physics of cell shading

Figure 2.5 shows an n-cell module with the one cell separated from the others for illustration purposes. The equivalent circuit of the separated cell is drawn using the model in Figure 2.3 while the other $(n-1)$ cells in the string are shown as a module with output voltage V_{n-1} and current I. In Figure 2.5 the separated cell is shaded and its current I_{SC} is reduced to zero. The only path for current flow is through R_P and the voltage drop across R_P causes the diode to be reverse biased and the diode current becomes zero. This entails that the current flowing in the entire module channels through R_S and R_P of the shaded cell. This however implies that the shaded cell reduces the output voltage instead of adding to it due to the voltage drop across R_S and R_P.

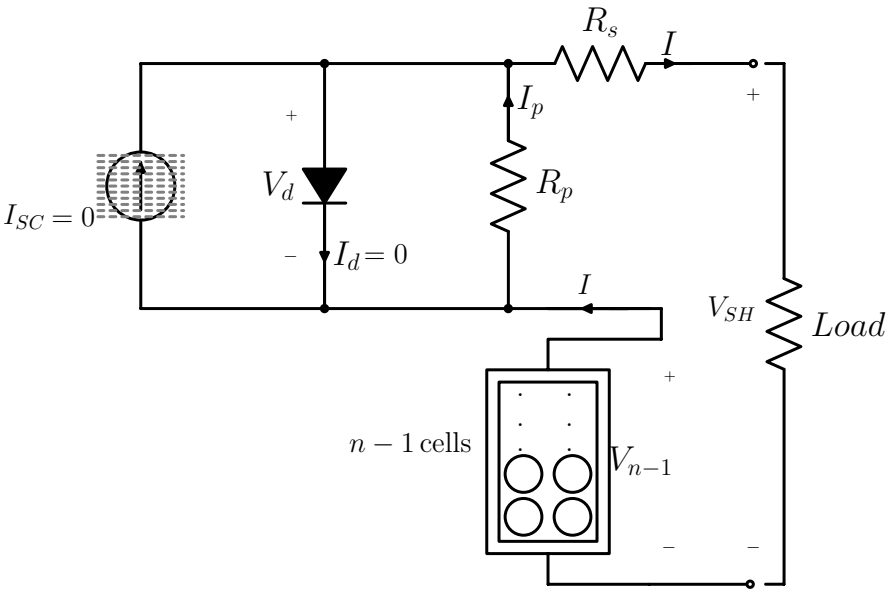

Figure 2.5: Module with one cell completely shaded

From Figure 2.5, it is shown that the output voltage of one-cell shaded module produces the output voltage V_{SH} given by Equation 2.3.6.

$$V_{SH} = V_{n-1} - I(R_P + R_S) \tag{2.3.6}$$

The output voltage V_{n-1} across the unshaded cells is described by Equation 2.3.7, where V is the output voltage when all n cells are are exposed to the sun and carrying a current I.

$$V_{n-1} = \left(\frac{n-1}{n}\right) V \tag{2.3.7}$$

Combining Equation 2.3.6 and Equation 2.3.7 gives the Equation 2.3.8 that determines the output voltage of a one-cell shaded module.

$$V_{SH} = \left(\frac{n-1}{n}\right) V - I(R_P + R_S) \tag{2.3.8}$$

At any given current I, the voltage drop ΔV is given by the expression in Equation 2.3.9.

$$\begin{aligned} \Delta V &= V - V_{SH} \\ &= V - \left(\frac{n-1}{n}\right) V + I(R_P + R_S) \\ &= \left(\frac{V}{n}\right) + I(R_P + R_S) \end{aligned} \tag{2.3.9}$$

In a case where the single cell has 50% of its area shaded whilst the rest of the cells are exposed to sunlight, as shown in Figure 2.6, the short circuit current of the single cell

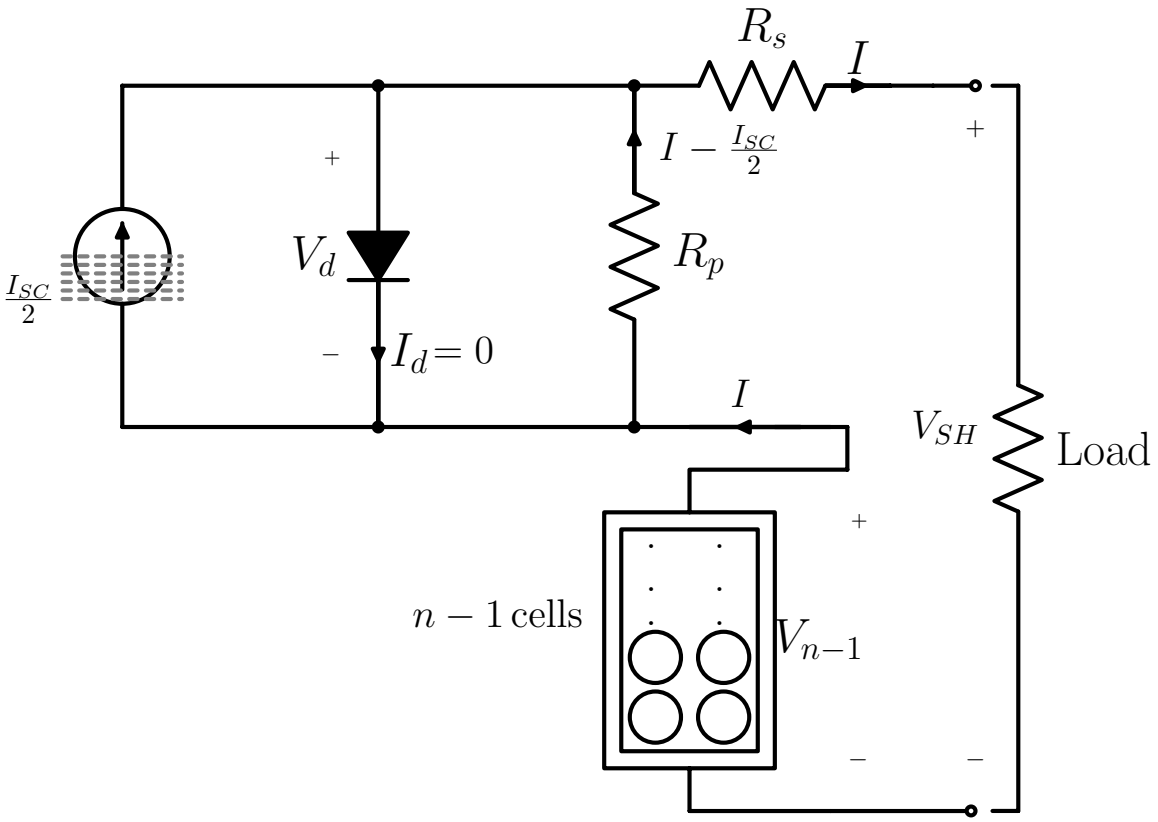

Figure 2.6: Module with one cell half-shaded. Current I exceeds $\frac{I_{SC}}{2}$

is halved to $I_{SC}/2$. However, if the current I that flows to the partially shaded cell from rest of the module is more than $I_{SC}/2$, the current equal to the differences between the two currents is channelled through the resistor R_P, as shown in Figure 2.6. The voltage drop across the resistor R_P, causes the diode to be reverse biased. This results in the total voltage of the entire module to be reduced according to Equation 2.3.10 where ΔV is the reduction in voltage at any given current I due to the shaded cell.

$$\Delta V = \left(\frac{V}{n}\right) + \left(I - \frac{I_{SC}}{2}\right)(R_P + R_S) \tag{2.3.10}$$

Moreover, the large current that is channeled through R_P, causes enormous power dissipation across R_P. The dissipated power results in hot spots generation on a small area and causing destructive effects such as degradation of the solar cell and the melting of solder.

2.3.2.2 Shade mitigation using Bypass and Blocking diodes

One way to mitigate the voltage-drop problem discussed previously due to cell shading is to connect a bypass diode across each cell in the module as shown in Figure 2.7. When

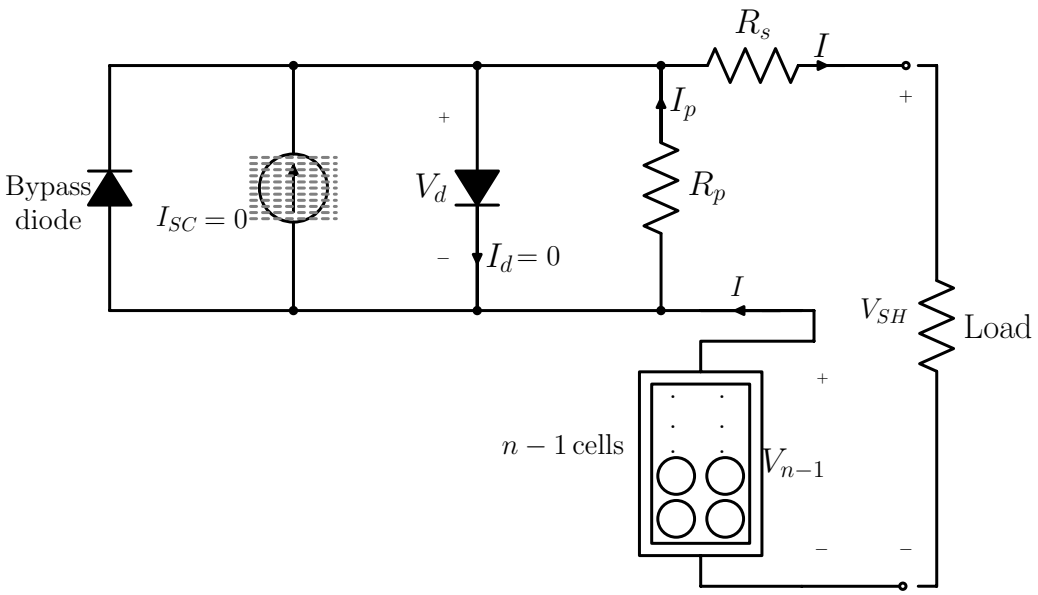

Figure 2.7: One-cell shaded module implementing bypass diodes

the cell is exposed to the sun i.e without any shading, voltage rise across the cell and the bypass diode is reverse biased. When the solar cell becomes shaded, the bypass diode is turned on, providing a current path around the shaded cell [8]. An ordinary diode has a voltage drop of about 0.6 V and therefore the bypass diode controls and limits the voltage drop across the shaded cell to 0.6 V instead of an enormous amount of voltage that could have otherwise been dropped without it. However, connecting a bypass diode across every cell is considered by manufactures as being not financially feasible and therefore a bypass diode is connected across a number of e.g one diode for every eight cells. Furthermore, employing a bypass diode across a cell or a string of cells prevents development of hot spots on shaded cells as current is channelled through the bypass diode instead [9, 10].

When strings of modules are wired in parallel, problem arises when one of the modules is not performing. Instead of the string with a non-performing module to supplying current, it rather withdraws current from the rest of the array [11]. This reduces the overall performance of the array. In order to avoid current being drawn by the non-performing string, blocking diodes also called isolation diodes, are connected in series with every sting as shown in Figure 2.8. So whenever strings are connected in parallel to each other, blocking diodes are connected in each of the parallel branch. Moreover, the blocking diodes also prevent the fully charged batteries from discharging at night when the array is not producing any power. Therefore the use of bypass and blocking diodes, improves the overall performance of an array.

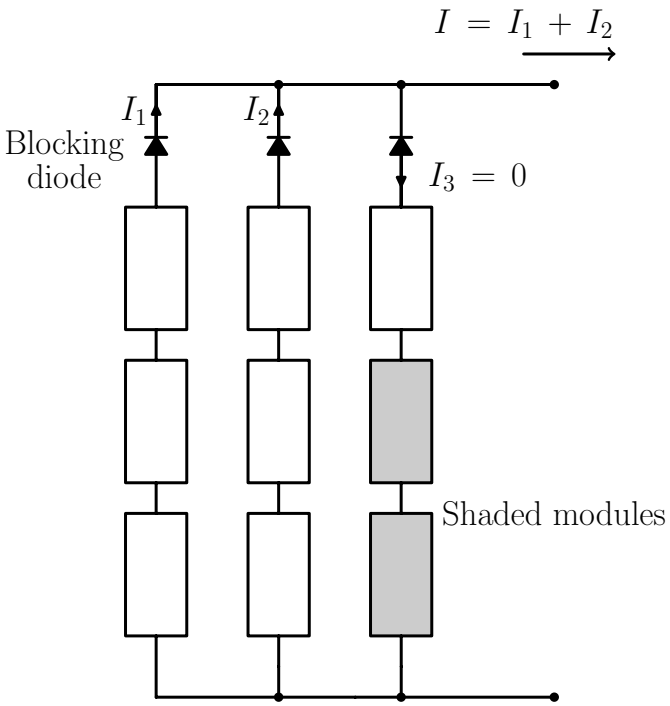

Figure 2.8: Array implementing blocking diodes to prevent reverse current flowing to the shaded string

2.4 Algorithms implemented by photovoltaic power electronic systems

The power transfer efficiency in PV systems depends on the impact of the environment conditions on the solar photovoltaic module and the electrical characteristics of the load. As the environmental conditions inevitably varies, the load characteristics that ensures the highest power transfer also changes. Different algorithms have been developed that control the load characteristics to keep the power transfer at highest efficiency. The Solar Array Emulator (SAE) system proposed in this project serves as a technological system that evaluates the performance of the control algorithms that changes the load characteristics to ensure maximum power transfer. A brief description of the different kinds of control algorithms are is given below.

2.4.1 Perturb and observe

The perturb and observe control strategy, also called the hill climbing method, operates by adjusting the output voltage of the PV array and measuring power delivered. If the measured power increases, further adjustments to the PV array's output voltage are made in that direction until the measured delivered power no longer increases [12]. If the

adjustments to output voltage decreases the delivered power, then the next adjustments are made in the reverse direction. This method is mostly used due to its ease of implementation and ensures top level efficiency provided that a proper predictive and adaptive hill climbing technique is used [13].

2.4.2 Incremental conductance

This method is based on the fact that the gradient of the power versus voltage curve is zero at maximum power point. By using this technique, the controller measures the incremental changes in PV array current and voltage to predict the effect of a voltage change. It utilizes the incremental conductance ($\Delta I/\Delta V$) of the photovoltaic array to compute the sign change in power with respect to voltage ($\Delta P/\Delta V$). The maximum power point can be found by incrementing the duty cycle of the converter until the ratio of the incremental changes ΔI and ΔV equals I/V [14]. The controller maintains the operating point at maximum power point until the non-linear I-V output characteristics changes due to changes in environmental conditions. Therefore, the control algorithm searches for a new maximum power point.

2.4.3 Constant voltage technique

This method is also called fractional open-circuit voltage method whereby the voltage is maintained to some percentage of the measured open circuit voltage under all operating conditions. This method is not a maximum power point tracking technique but is implemented in cases where MPPT techniques do not work or rather when a simple and in-expensive method is the only available option. During operation of the constant voltage method, the power delivered to the load is momentarily interrupted and the open-circuit voltage with zero current is measured. The controller resumes operation by regulating the voltage to a fixed ratio such as 0.76, of the open circuit voltage V_{OC} [15]. The operating point of the PV is thus kept near the maximum power point by regulating the array voltage and matching it to the fixed reference voltage of $V_{ref} = kV_{OC}$ where k is the fixed ratio. Although the method is simple and low cost, the interruptions, reduce array efficiency and the operating point is not really the maximum power point of the array.

2.5 Existing designs of solar array emulators

In this section, the designs of existing solar array emulators are presented. Several models have been developed that emulate the behaviour of actual photovoltaic arrays. However,

the different models developed have the sole purpose of evaluating and certifying the performance of photovoltaic systems such as grid-tie inverters, maximum point trackers and battery chargers.

2.5.1 2-stage solar array emulator

The solar array emulator developed in [16] has a structure that is shown in Figure 2.9 and is based on Digital signal processing (DSP). The system has two stages namely the AC/DC stage and the DC/DC stage. The AC/DC stage is a rectifier stage based on a three phase pulse-width modulator (PWM) converter. The converter is synchronised with the grid based on a Phase-Locked-Loop technique that has good responses for voltage unbalances and voltage harmonics [17]. The modulation strategy implemented by the AC/DC stage is a space vector PWM (SVPWM). This stage is responsible for generating the DC bus voltage of the emulator from the grid. The DC/DC stage of the system, operates in two modes. The first mode is the open-circuit control mode that is responsible for starting the converter switching operation and controlling the output voltage when the system is unloaded. The second mode is the emulator control mode. It operates based on the control strategy shown in Figure 2.10. The control mode is based on a an I-V curve look up table created for specific temperature and irradiation conditions. The output voltage measurement is interpolated in the look up table on order to get the corresponding inductor reference current. The interpolation process is dynamic thereby permitting the system to emulate the characteristics of a PV module [16] .

2.5.2 DSP controlled solar array emulator

The block diagram of the solar array emulator developed in [18], is shown in Figure 2.11. The system implements a DC/DC buck converter for voltage regulation. A voltage control strategy with pulse-by-pulse limitation technique is employed in order to control the converter. The converter is powered by a laboratory DC power supply and it is also connected to a programmable DC load. The system operates in two different modes namely the table mode and the basic mode. The basic mode implements only four parameters obtained from a PV module datasheet such as I_{sc}, V_{oc}, V_{mp} and I_{mp} to create the I-V profile based on a developed algorithm. The table mode on the other hand requires as many as possible current-voltage pairs either extracted from a datasheet or obtained experimentally. The I-V profile to be emulated from either mode is then is loaded from the PC into the DSP board using Labview software via RS-232 serial communication interface. The I-V profile received by the DSP is stored in a look up table after appropriate scaling [18].

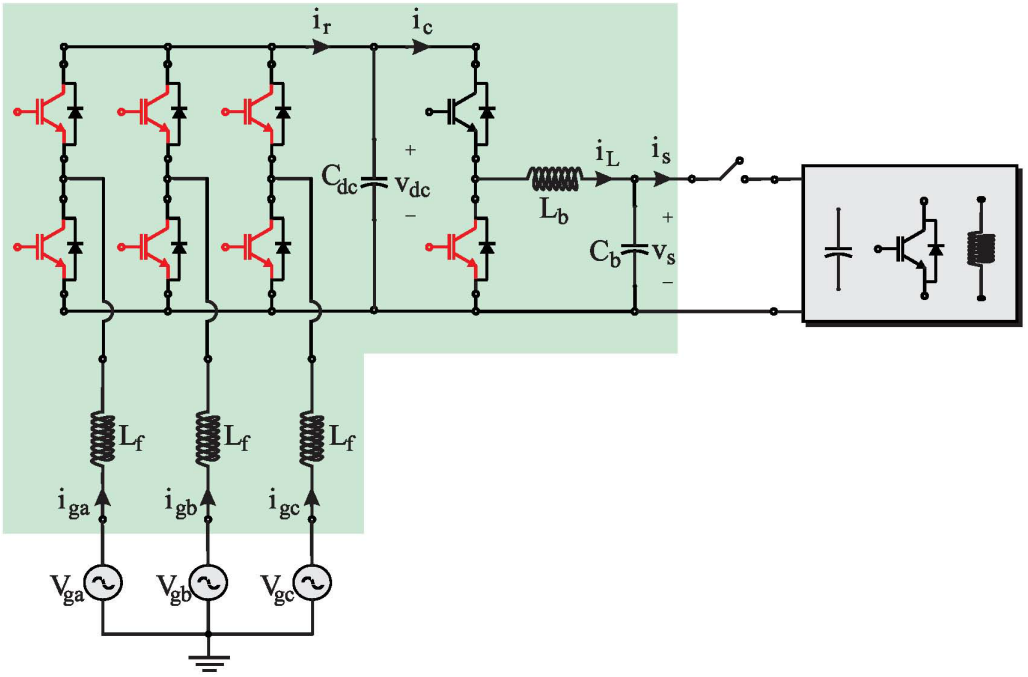

Figure 2.9: AC/DC stage connected to the DC/DC stage with a PV inverter stage to be evaluated, connected as the load [16]

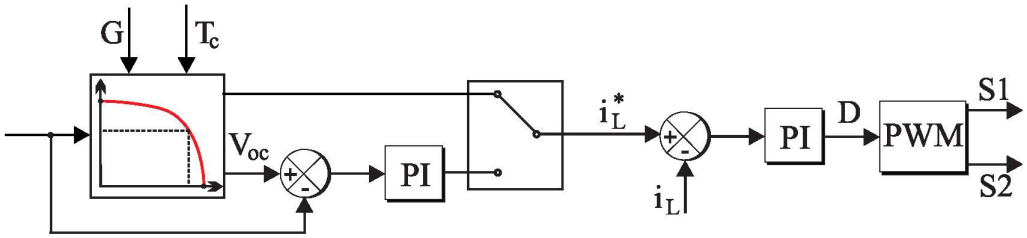

Figure 2.10: Control strategy of the DC/DC converter stage [16]

The system performs the emulation process according to the block diagram in Figure 2.12. The buck converter output current is measured by the analog-digital A/D converter and the measured value is stored in the look up table after scaling. The measured current searches through the LUT in order to find the corresponding reference voltage, as illustrated in Figure 2.12. The reference voltage signal and the sampled actual output voltage are compared to each other and the error is processed by the controller. Thus the system in Figure 2.11 implements a voltage control strategy in order to emulate an I-V characteristic curve [18].

2.5.3 Voltage and current mode controlled solar array emulator

The solar array emulator developed in [19], is based on the simple block diagram in Figure 2.13. The system is DSP controlled and consists of a 2 kW step-down DC/DC

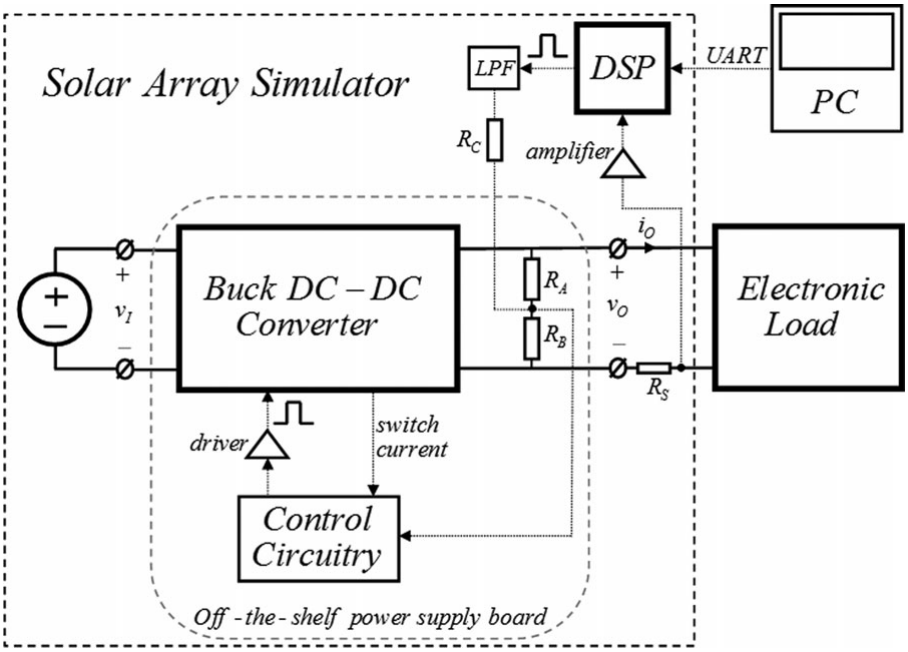

Figure 2.11: Block diagram of the DSP controlled SAS prototype system [18]

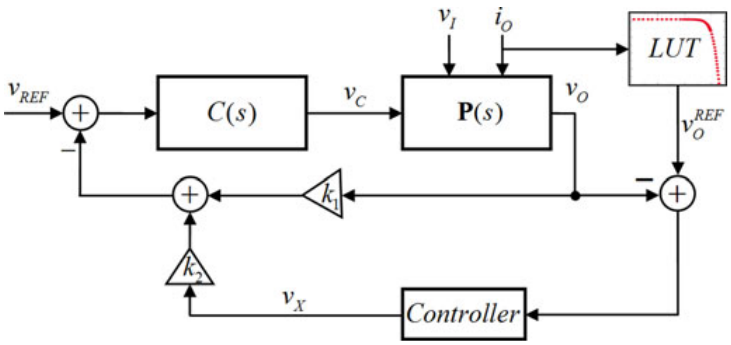

Figure 2.12: DSP voltage control strategy [18]

power converter. The bus voltage is generated by the rectifier, as shown in Figure 2.13. The hybrid control strategy for the emulator is implemented on the DSP board and moreover the DSP board is responsible for communication and A/D measurements. The emulator implements two control modes, namely the voltage control mode and the current control mode. The maximum power point of an I-V curve corresponds to a critical resistance R_c. The emulator system is designed in such a way that if the equivalent load R_L of the emulator system is greater than R_c, the voltage control mode operates effectively and if the R_L is less that R_c, the current control mode is used effectively. The operation between the two modes is divided by the load line of R_c as shown in Figure 2.14. If the voltage control mode is operating, the output current is measured and by looking in the current-voltage LUT, the controller will select a voltage reference and then adjust the PWM duty cycle in order to produce the right voltage. Similarly, if the

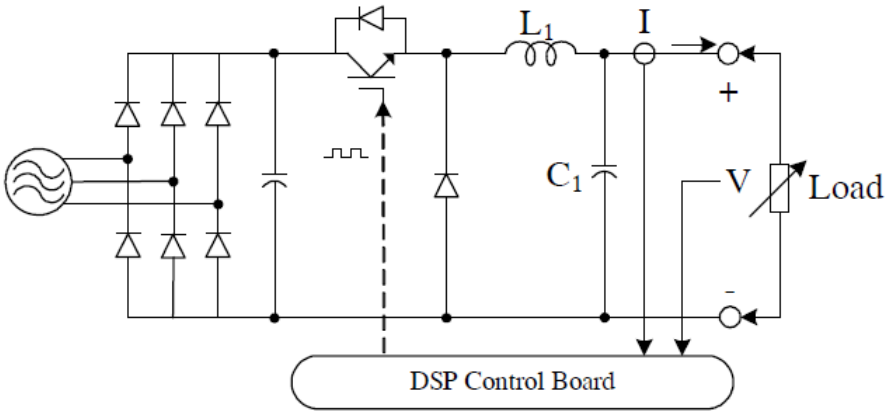

Figure 2.13: Block diagram representation of the DSP controlled solar array emulator [19]

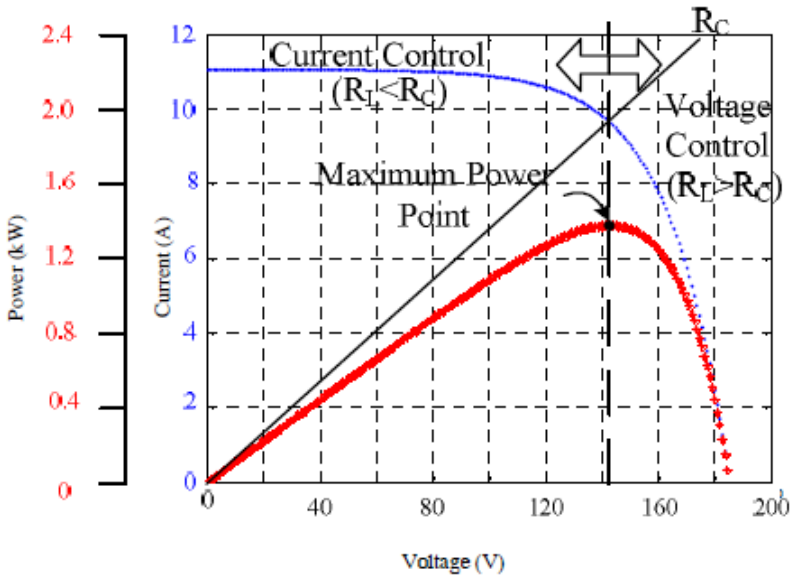

Figure 2.14: Distinction between the regions where the current and voltage control modes operate [19]

current control mode is in operation, the output voltage is measured and by looking in the LUT, the controller selects the current reference and adjusts the PWM duty cycle in order to regulate the current. Therefore the interchange between the two modes enables the system to emulate the I-V curve effectively as shown by the practical results in [19].

2.6 Commercial solar array emulator

The emulator shown in Figure 2.15 is a programmable 62000H-S model Solar Array Emulator that can emulate a PV array up to a maximum open circuit voltage V_{oc} of 1000 V and

Figure 2.15: Chroma 62000H-S model Solar Array Emulator [20]

short circuit current I_{sc} of 25 A [20]. The price for the system on Ebay is approximately ZAR 113,274.90. The system has high speed and precision digitising voltage and current measurement circuits with a 100 kHz A/D converter. The system employs a graphical user interface (GUI) through digital interfaces such as USB, Ethernet or RS232 communication ports. This allows the user to easily define the V_{oc}, I_{sc}, V_{mp} and I_{mp} parameters that can be used to create I-V characteristic curves. Moreover, the system allows the user to define the operating weather conditions such as irradiation, temperature, rain and shading by trees or clouds, which affects the I-V output characteristics [20].

This emulator is ideal for evaluating the maximum power tracking algorithms implemented by a PV inverters under different operating conditions. The emulator also verifies the high/low limit of operating input voltage for PV inverters. Moreover, the system verifies the maximum power point tracking performance of inverters for a period spanning from morning to nightfall.

2.7 Summary

In this chapter, relevant background literature on photovoltaics is discussed. The physics involved in converting sunlight energy into electricity is discussed . Two PV cell equivalent models are presented and the limitation of the simple model under shading conditions is also discussed. An explicit solution that characterises the non-linear current-voltage relationship of a photovoltaic cell is derived. Moreover, the solution is used to simulate the I-V characteristic curve of series connected PV cells. The effects of environmental condi-

tions such as shading, temperature and irradiation are also discussed. Relevant equations that characterise the effects of the environment conditions on the I-V characteristic curve are also derived. Moreover, the mitigation strategies against the effects of shading are also presented. Published articles on solar array emulators are discussed as well as the methodologies they implemented in order to successfully emulate the characteristics of an actual photovoltaic array. Furthermore a commercially available emulator is discussed.

Chapter 3

Solar Array Emulator Overview

The Solar Array Emulator (SAE) system is designed to operate in two modes namely the simulation and the emulation mode. In the simulation mode the SAE system employs a developed graphical user interface (GUI) to simulate the current-voltage (I-V) and power-voltage (P-V) characteristic curves of a photovoltaic (PV) module. The GUI running on a personal computer (PC) allows the user to select the operation mode and also allows the user to define the module's parameters e.g short circuit current I_{sc}, open circuit voltage V_{oc} and the number of cells. Moreover the user defines the module's operating environmental conditions e.g. ambient temperature, irradiance level and percentage shading or percentage uniform accumulation of dust on the module. The user can also specify the number of connected modules in parallel and in series in an array configuration. An algorithm running on the PC then interprets the user-defined specifications based on the equations derived in Chapter 2, in order to simulate the corresponding I-V and P-V characteristic curves. The SAE system executes the simulation mode as shown in the flow diagram in Figure 3.1 and plots the simulated curves on the GUI. An analysis of the I-V and P-V characteristic curve simulated in the simulation mode under different user-defined specifications will be discussed in more detail in Chapter 6.

The SAE system running in the emulation mode, is utilised as a controllable in-door test system that emulates the characteristics of an actual PV module/array and evaluates the characteristics and performance of the connected load. The load is connected to a synchronous DC/DC converter power supply. The converter is responsible for current regulation based on the pulse width modulation (PWM) principle. The modulation process is controlled by the current control algorithm running on the FPGA board. The FPGA board is the central subsystem of the SAE system and is discussed in detail in Section 3.1. Moreover the hardware design of the synchronous DC/DC converter is discussed in Chapter 4 and the strategies implemented in designing the current controller are discussed in Chapter 5.

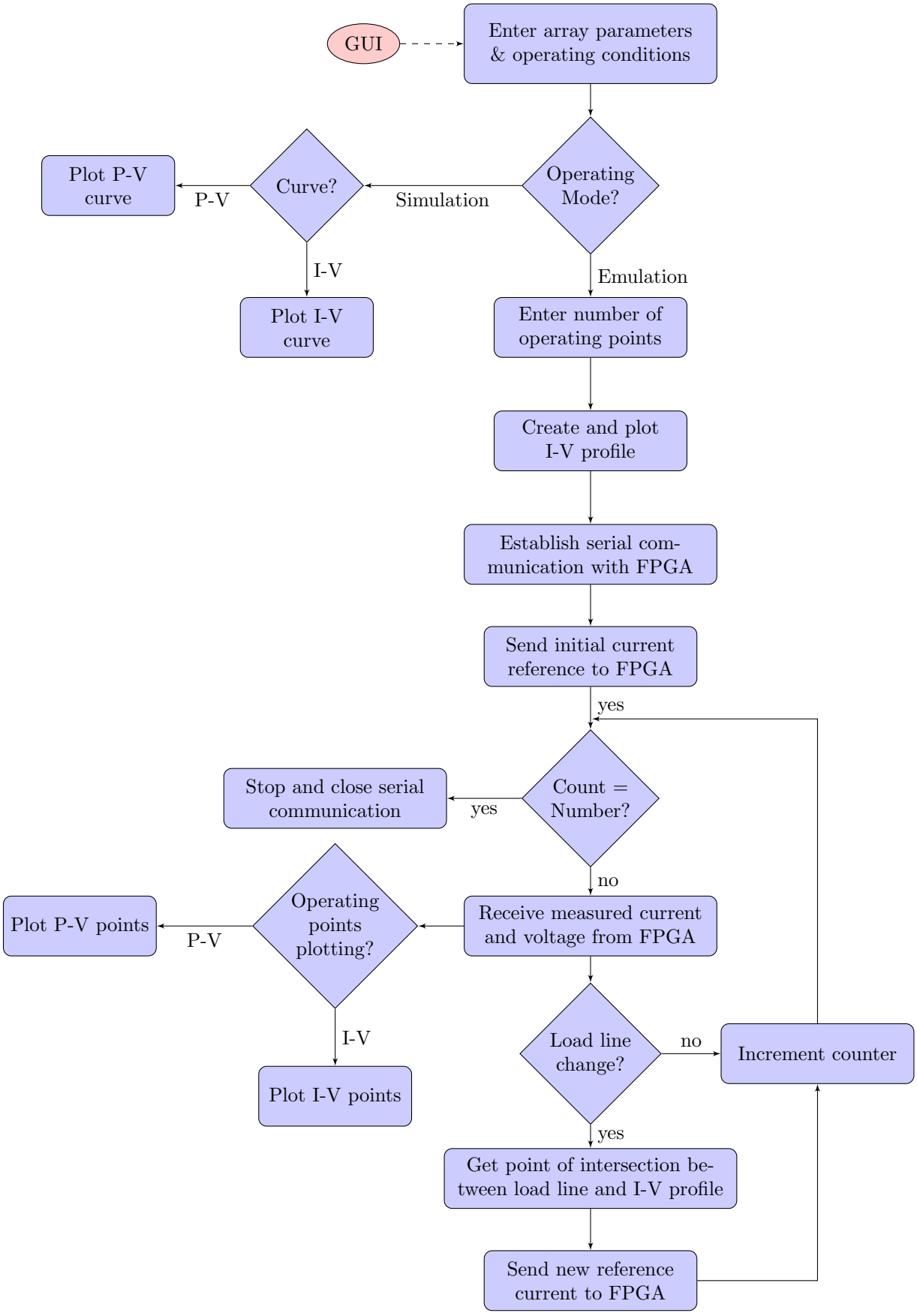

Figure 3.1: SAE system operations flow diagram

For this project, the connected load systems under test and evaluation are the grid-tie inverter, maximum power point tracker (MPPT) active load and a variable resistor. In the emulation mode, the SAE system employs the GUI to enable the user to define the array configuration, module parameters and the operating environmental conditions. If the user selects the emulation mode, it is executed as shown by the flow diagram in Figure 3.1 and an illustration example of how the emulation mode operates is discussed in Section 3.2.1. For the case of the connected load being either the MPPT active load or grid-tie inverter, the SAE system evaluates the performance of load's power electronic circuit and its corresponding control algorithm, based on the load's I-V operating points along the theoretical I-V profile created. Practical experiments in the emulation mode are conducted and discussed in greater detail in Chapter 7. The SAE system is rated at 20 kW with a maximum current of 18 A and a maximum voltage of 900 V and therefore the system is designed to emulate an array with a maximum current and voltage that falls within the specified limits.

In order for the SAE system to function according to the flow diagram in Figure 3.1, power electronic hardware systems are designed and the software algorithms that provide control and monitor the hardware systems are developed. In this chapter, the design of the software algorithms are discussed in greater detail.

3.1 The Field-Programmable Gate Array (FPGA) device

The FPGA unit used in this project is a DE1-SoC development board that is equipped with high speed memory, video and audio capabilities, ethernet networking etc. It is based on a Cyclone V SoC 5CSEMA5F31 device with 85 000 programmable logic elements, 4450 Kbits embedded memory and the system clock is 50 MHz. The FPGA device is configured through a download cable by means of the JTAG interface [21].

The FPGA technology is flexible, complex and enables fast parallel signal processing and the device is programmed in VHDL. The FPGA devices makes it possible for analog control loops to be emulated in the digital domain. This is achieved by the FPGA device's ability to oversample signals at rates significantly higher than the switching frequency of the DC/DC converter. The sampling rates are usually 1000 times the switching frequency and therefore the digital control loop and the pulse width modulator are updated at every sampling instant. This type of implementation using the FPGA device, enables digital control loops to closely emulate analog control loops. Therefore, transport delays inherent in regularly-sampled control loops, are eliminated. Due to these kinds of advantages posed

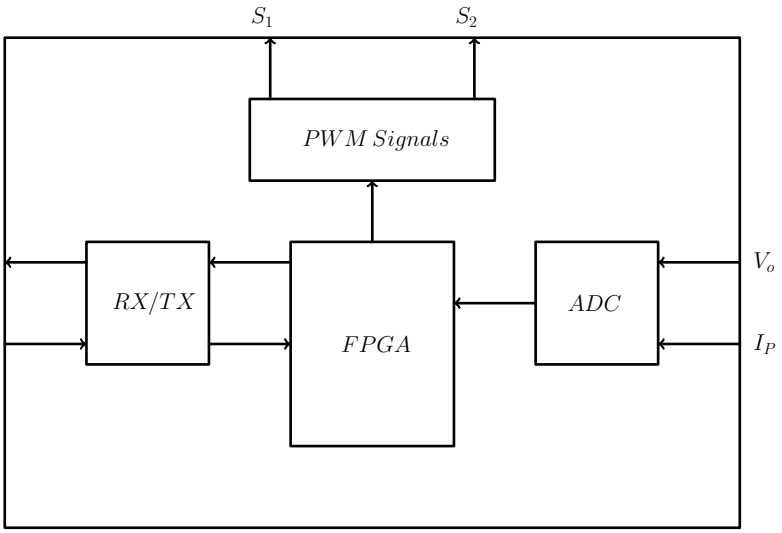

Figure 3.2: Functions of the FPGA board used

by the FPGA device, the device is chosen for implementation in this project

In this project, the SAE system utilises the FPGA device for universal asynchronous receiver/transmitter (UART) serial communication, generation of pulse width modulation (PWM) signals and current and voltage measuring using an 8-bit wide on-board A/D converter on the FPGA. The measured current and voltage values are transmitted to the PC via the serial communication interface. The PWM gate signals generated by the current control algorithm, controls the DC/DC switches labelled S_1 and S_2. The FPGA device is the central sub-system of the SAE system with its functions and set-up configuration shown in Figure 3.2.

3.2 Software Design

In this section, the development of the SAE system firmware is described. The technique employed by the SAE system in executing the emulation mode is explained in detail. Moreover, the algorithms running in the FPGA responsible for PWM generation, UART serial communication, analog to digital (A/D) conversion and current control are explained in greater detail.

3.2.1 Emulation technique

The user specifies the number of I-V operating points of the connected load that the SAE system should plot on the GUI. A theoretical I-V profile representing the profile of an actual array is created based on the user-defined specifications. A serial communication

interface is then established between the algorithm running on the PC and the current control algorithm running on the FPGA board. An initial reference current is transmitted to the FPGA board in order to initiate the current regulation process by the DC/DC converter power supply. The FPGA responds by transmitting the I-V operating points of the connected load to the PC. The algorithm on the PC plots the I-V operating point of the load and determines the load line characteristics of the connected load. If the load line is different from the previous one, a new current reference point that corresponds to the intersection point between the I-V curve and the load line is sent to the FPGA.

A suitable strategy is designed that is employed by the SAE system to emulate an I-V characteristic curve. For the sake of illustration, a constant resistive load is connected to the output terminals of the DC/DC converter. The SAE system is operated in emulation mode and it executes according to the flow diagram in Figure 3.1. The user-defined environmental conditions and module parameters are specified as; a temperature of 25 °C, irradiation of 1000 W m^{-2}, V_{oc} of 10 V and I_{sc} of 1.5 A. The user also specifies the number of operating points to be plotted and therefore the emulation mode only operates until the number of operating points specified is reached, then the process is stopped. A theoretical I-V characteristic curve representing the profile of an actual array is created based on the user-defined specifications. A serial communication interface is then established between the algorithm running on the PC and the current control algorithm running on the FPGA board. An initial reference current is transmitted to the FPGA board in order to initiate the current regulation process by the DC/DC converter. The FPGA responds by measuring the DC/DC converter's load voltage and current and transmitting these values to the PC via serial communication. The load voltage and current are related according to the linear characteristics of a load line shown in Figure 3.3. The point P_k shown in Figure 3.3, is the point of intersection between the load line and the theoretical I-V characteristic curve of the module with specifications defined by the user. The point P_k, corresponds to the new reference current $I^{\star}_{ref}$ that is transmitted to the FPGA board as a new reference current to the current control algorithm. The FPGA will continuously transmit the load voltage and current to the PC and these operating points are plotted on the GUI.

At each reference current, the SAE system's actual output load current I_{act} that corresponds with the operating point P_1, is constantly compared with the reference current $I^{\star}_{ref}$. Their difference is used by the current control algorithm to control the PWM gate signals that drive the DC/DC converter switches until a point of convergence is reached, that is at point P_k. Therefore the algorithm running in the FPGA device is responsible for constantly adjusting the PWM duty cycle so that the operating point of the DC/DC converter is moved from the point labelled P_1 to point P_k as shown in Figure 3.3. The

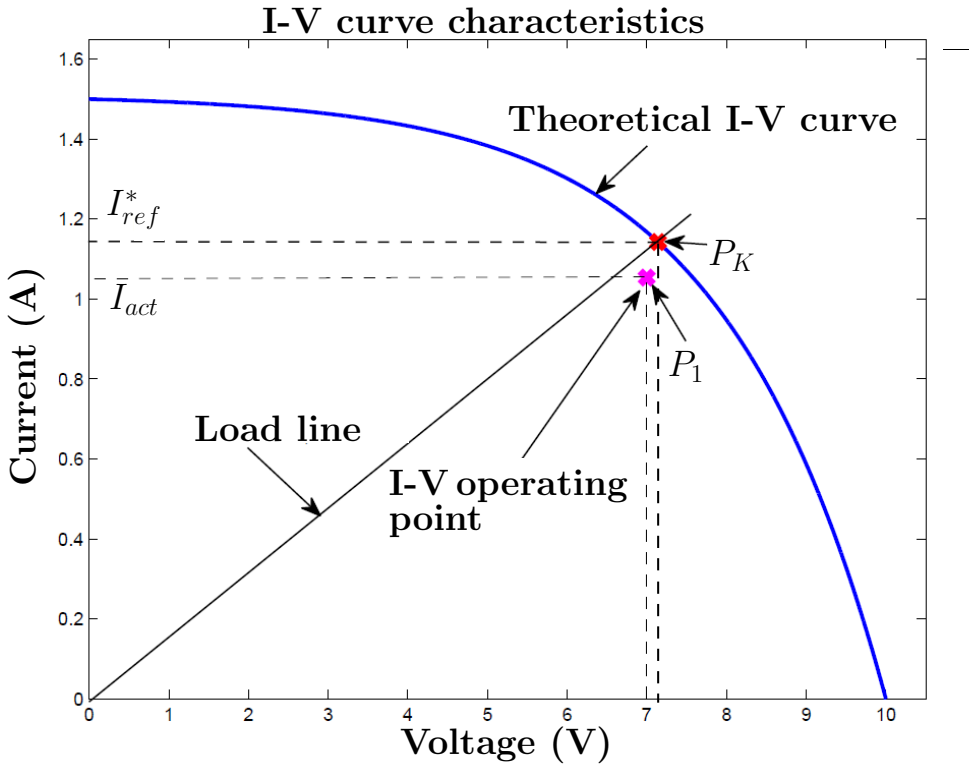

Figure 3.3: I-V characteristics curve emulation technique

FPGA regulates and maintains the operating point at P_k and at this point, the SAE system's operating point coincides with the point of intersection between the load line and the array's I-V characteristic curve, thereby successfully emulating the behaviour on an actual PV module.

3.2.2 Analog to digital (A/D) converter

The algorithm running on the PC continuously inquires measured current and voltage values from the FPGA device as illustrated in the flow diagram in Figure 3.1. Furthermore, the feedback control algorithm discussed in Section 3.2.4, running on the FPGA device implements measured current values for the current regulation process. The current and the voltage are measured using an A/D converter (AD7928) on the FPGA device. The converter (slave device) is an eight-channel 12-bit A/D converter with a serial interface compatible with the Serial Peripheral Interface bus (SPI). The SPI is the standard for communication between the A/D converter and the FPGA (master device). The reference voltage of the A/D converter is 5 V, giving a resolution of about 1.22 mV. Moreover, the converter is used to measure current and voltage on two different channels.

The algorithm to operate the A/D converter is designed according to the state machine

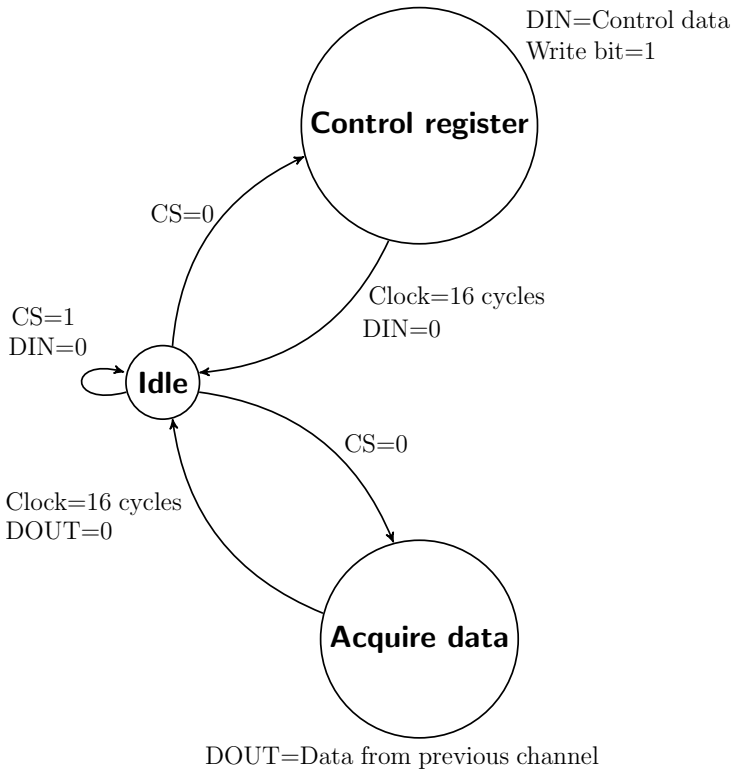

Figure 3.4: Analog to digital conversation state machine

in Figure 3.4. Figure 3.5 shows the serial interface timing diagram of the A/D converter. The signal *CS* represents the Chip Select logic input for initiating conversions in the A/D converter, and *SCLK* represents the Serial Clock logic input which provides the serial clock for accessing data from the converter and which is also used as a clock source for the conversion process. Moreover, *DIN* is the data to be written to the control register of the converter and *DOUT* is the conversion output serial data stream. Based on the timing diagram in Figure 3.5, when the A/D algorithm running on the FPGA pulls the *CS* low, the A/D converter initiates the conversion process [22]. Data indicating the selected channel, analog input range, output coding and the write bit are loaded from the *DIN* pin onto the control register on the falling edge of *SCLK*. The data transferred in the *DIN* line corresponds to the converter configuration for the next conversion. The resulting conversion is provided as a serial data stream on the *DOUT* line. The bits are clocked out of the *DOUT* line on the falling edge of *SCLK*. The output data stream starting with the most significant bit (MSB), is made up of one leading zero, three address bits which indicates where the conversion result belongs to and then followed by 12 bits of the conversion data. Therefore sixteen clock cycles are required to complete the conversion and access the conversion result. After the sixteen clock cycles, there is a wait period in which *DOUT* goes into a high impedance state and *CS* can then idle high until the

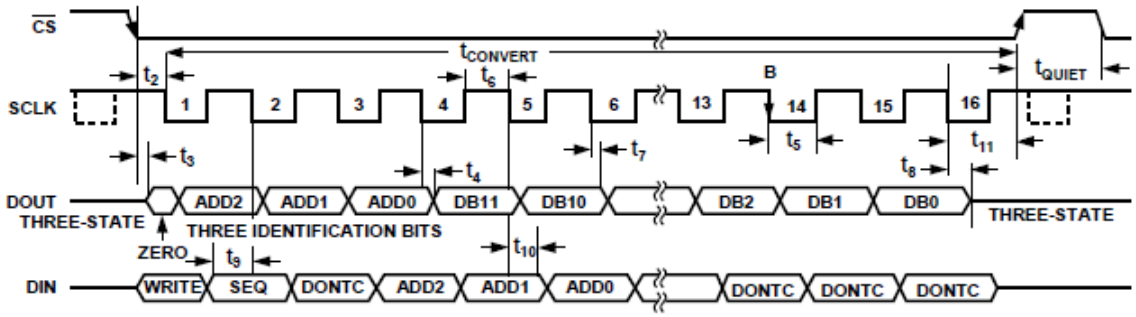

Figure 3.5: Serial Interface Timing Diagram [22]

next conversion is initiated. After every sixteen clock cycles, the channel to be converted is changed between the channel responsible for current and the channel responsible for voltage measurements.

3.2.2.1 A/D converter experimental test

The current controller designed and detailed in Chapter 5 was implemented on the FPGA board in order to regulate a current of 2 A flowing in the inductor of the DC/DC converter. In order to measure the inductor current and the load voltage, the AD7928 A/D converter is used. In order to visualise the samples of the measured data over a period of time, a debugging tool on the FPGA's Quartus® programmer software called the SignalTap® II Logic Analyzer is implemented. This logic analyser solution allows the user to examine the internal signals' behaviour without the use of extra input/output (I/O). These internal signals are examined while the algorithm on the FPGA is still running [23]. It captures the signal data of the internal nodes or the I/O pins and stores the data in the device memory.

In this case, the inductor current and load voltage measurements measured by the A/D converter are captured using the logic analyse and the Matlab® software is used to visualise and plot the measured data. Figure 3.6 shows an average inductor current of approximately 2 A and Figure 3.7 shows an average load voltage of approximately 15.25 V when load connected is 7.8 Ω. However random spikes are observed when taking both measurements as shown in Figure 3.6 and Figure 3.7. A maximum current percentage deviation $\epsilon_I(\%)$ of 26.5% is calculated using Equation 3.2.1 where $I_{avereage}$ is the average measured current and I_{spike} is the maximum measured current spike. Moreover a maximum voltage percentage deviation $\epsilon_v(\%)$ of 3.8% is calculated using Equation 3.2.2 where $V_{avereage}$ is the average measured current and V_{spike} is the maximum measured voltage

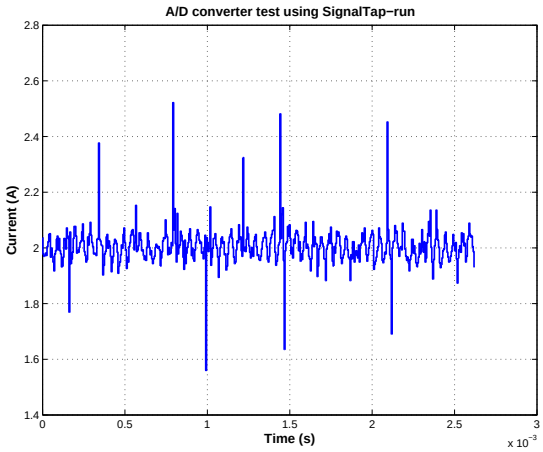

Figure 3.6: Inductor current measured using A/D converter

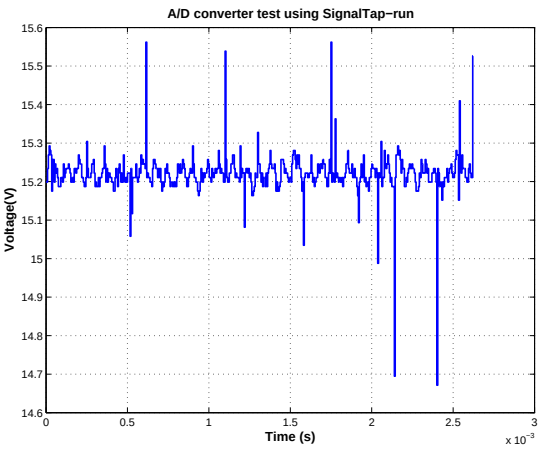

Figure 3.7: Load voltage measured using A/D converter

spike.

$$\begin{aligned}\epsilon_I(\%) &= \frac{|I_{avereage} - I_{spike}|}{I_{avereage}} \times (100\%) \\ &= \frac{|2 - 2.53|}{2} \times (100\%) \\ &= 26.5\%\end{aligned} \tag{3.2.1}$$

$$\begin{aligned}\epsilon_V(\%) &= \frac{|V_{avereage} - V_{spike}|}{V_{avereage}} \times (100\%) \\ &= \frac{|15.25 - 14.67|}{15.25} \times (100\%) \\ &= 3.80\%\end{aligned} \tag{3.2.2}$$

Based on the calculated percentage deviations, it can be observed that the occurrence of the random spikes reduces the integrity of the measured data. Several other tests are conducted and such spikes are still be observed. Moreover, several measures are taken to reduce the noise caused by the switching circuits i.e. power supply circuit and the DC/DC converter. This is done in order to improve the accuracy of the measurements. The occurrence of the spikes is not completely eliminated and thus the occurrence of spikes is attributed to the non-ideal performance of the AD7928 A/D converter, noise from the switching circuits and noise from the surrounding circuits. However such effects due to the occurrence of random spikes affects the practical measurements as shall be observed and discussed in Chapter 7.

3.2.3 Serial port communication

The control algorithm running on the FPGA device continuously communicates with the algorithm running on the PC via the UART serial communication port interface. The algorithm running on the PC transmits current reference $I^{\star}_{ref}$ to the FPGA and in return the FPGA transmits current-voltage operating points of the load to the PC. The bidirectional serial communication interface enables transmission and reception of data between the FPGA device and the PC. In order to implement the serial communication using the FPGA, two discrete functional components namely the Transmitter and Receiver responsible for transmission and reception of data are designed in the VHDL language. The components are included and port mapped in the main entity i.e current control architecture.

The transmission line consists of just one single wire and holds a HIGH state while it is idle. When the intention to transmit data arises, the wire holds a LOW state, signalling the start of the transmission. This is why the first bit that is transmitted is called the *START* bit as shown in Figure 3.8. The HIGH state of the transmission line corresponds to the logic 1 and LOW state corresponds to logic 0. After the *START* bit has been sent, the 8-bit data i.e in this case either a voltage or a current is transmitted. After the 8-bit data transmission is finished, a STOP bit with a logic 1 is transmitted. After the STOP bit has been transmitted, the transmission line remains in the idle state until the next available communication as shown in Figure 3.8. Likewise, the reception line awaits data coming and evades the *IDLE* state as soon as there is new data available. The reception line verifies the start and stop bit logic states to ensure that there are no frame errors as the data is bring received. Therefore each data package is 10-bit wide, 8-bits being the data and the other two being the start and the stop bit, as shown in Figure 3.8. The data transmission and reception strategies are described fully in the following sections using finite state machines.

3.2.3.1 Transmission

The transmission finite state machine in Figure 3.9 is responsible for sending current and voltage measurements from the FPGA to the PC. The state machine operates at a clock frequency of 50 MHz. The new transmission process will only start if there is no communication currently running i.e. if the transmission flag, TX_FLG=0, the start signal $START$=1 and the $BUSY$=0. The *START* bit indicates the start of the transmission process and the *BUSY* signal indicates whether or not the transmission line TX_LINE is busy. The parallel data to be sent, *DATA*, is transferred to the transmit data register *DATAFLL* vector between the start bit *DATAFLL(0)* and the stop bit *DATAFLL(9)*.

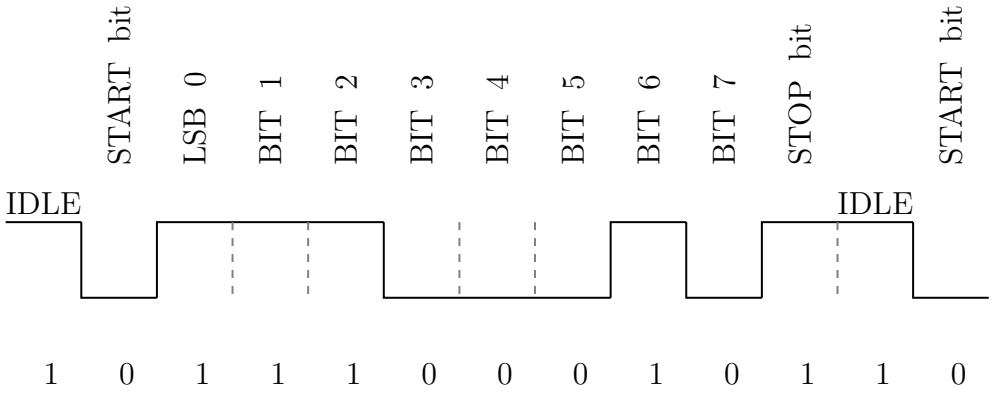

Figure 3.8: Transmitted or received data frame

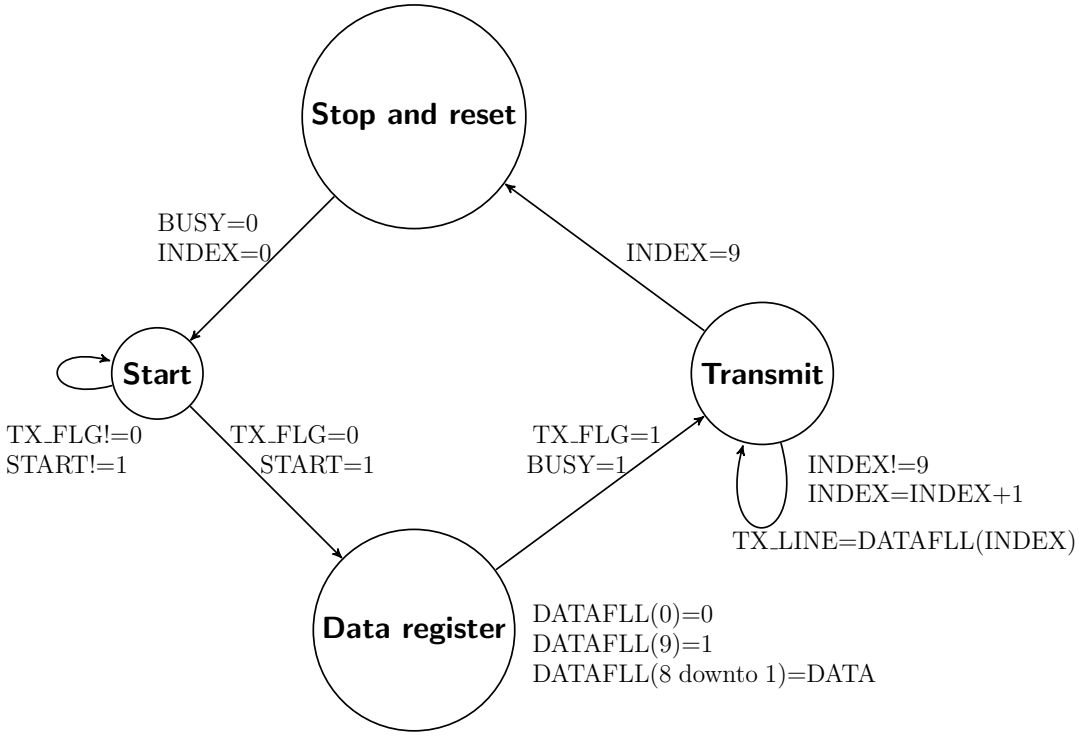

Figure 3.9: The signal transmission state machine

The bit rate for the UART communication is 9600 Bit/sec and a counter is specifically defined which counts up to 5208, in order to achieve the desired bit rate. The maximum value of the counter is calculated using Equation 3.2.3.

$$\begin{aligned} Count &= \frac{Clock\ frequency}{Bit\ rate} \\ &= \frac{50\,\text{MHz}}{9600\,Bit/sec} \\ &= 5208 \end{aligned} \tag{3.2.3}$$

If the desired bit rate is achieved and the signal TX_FLG is set to logic 1, the data in the transmission data register, $DATAFLL$ vector is transferred to the transmission shift register, TX_LINE which transmits the bits one by one. An $INDEX$ counter is used that selects which bit is transmitted at a time. The $INDEX$ counter, increments by one until the ninth bit i.e. the stop bit is sent, indicating the completion of the transmission process. When the transmission process is finished, the signals TX_FLG , $INDEX$, $BUSY$ and $START$ are reset to default logic states.

3.2.3.2 Reception

The current reference values sent by the algorithm running on the PC are received by the FPGA through the use of the designed signal reception finite state machine depicted in Figure 3.10. The reception process starts if no communication is active i.e. RX_FLG=0, $BUSY$=0 and the RX_LINE is in LOW state, that is when start bit is detected. If all the conditions are true, RX_FLG and $BUSY$ are set to logic 1. The $INDEX$ counter is used to determine the index value of the bit currently being received. While the reception process is running, the available bit on the reception line, RX_LINE is assigned to the corresponding bit $INDEX$ value in the receiver data register, $DATAFLL$ vector. The $INDEX$ value increments by one at a time and when it is equal to 9, the reception process is complete as all the data has been received. After completion, the first and the last bits are checked if they are in logic states 0 and 1, respectively. This is done to ensure that there are no frame errors incurred as the data is being transmitted from the other end. If the frame error test is passed, the signals RX_FLG and $BUSY$ are set to default values.

3.2.4 PI Controller and modulator

The current control algorithm running on the FPGA device is based on a Proportional Integral (PI) controller. The continuous time-domain PI controller is converted to its

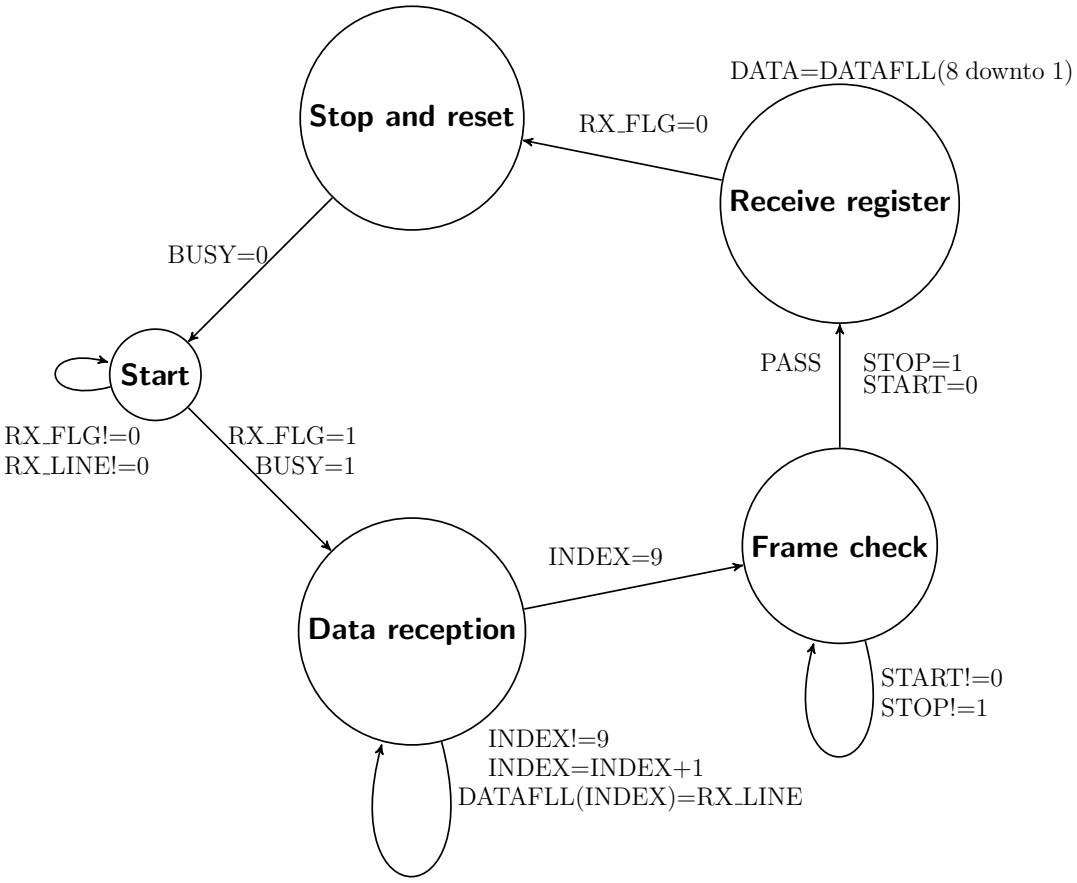

Figure 3.10: The signal reception state machine

discrete time equivalent using the impulse invariant transform in order to be implemented in the FPGA. The design and the implementation of the PI controller will be discussed in greater detail in Chapter 5. Figure 3.11, shows how the PI controller and the pulse width modulator are employed for current control using the FPGA device. The PI controller algorithm is developed based on the block diagram in Figure 3.11. The PI controller continuously calculates the error signal i.e. the difference between the reference current and the measured current. The error signal is processed in different and parallel stages namely the proportional gain stage and the integral stage. The proportional gain stage only considers the current size of the error signal at the time of controller calculation and the error signal is multiplied with the proportional gain K_p . However the integral stage considers the history of the error signal and how much it deviates from the reference signal over time. An accumulator shown in Figure 3.11 carriers out the integration process and the error signal is multiplied by the integral gain K_i, before the product is integrated by the accumulator. In other words the accumulator sums up the complete error history up to the present time, beginning from the time the controller started running. The accumulator operates at a clock frequency of 50 MHz.

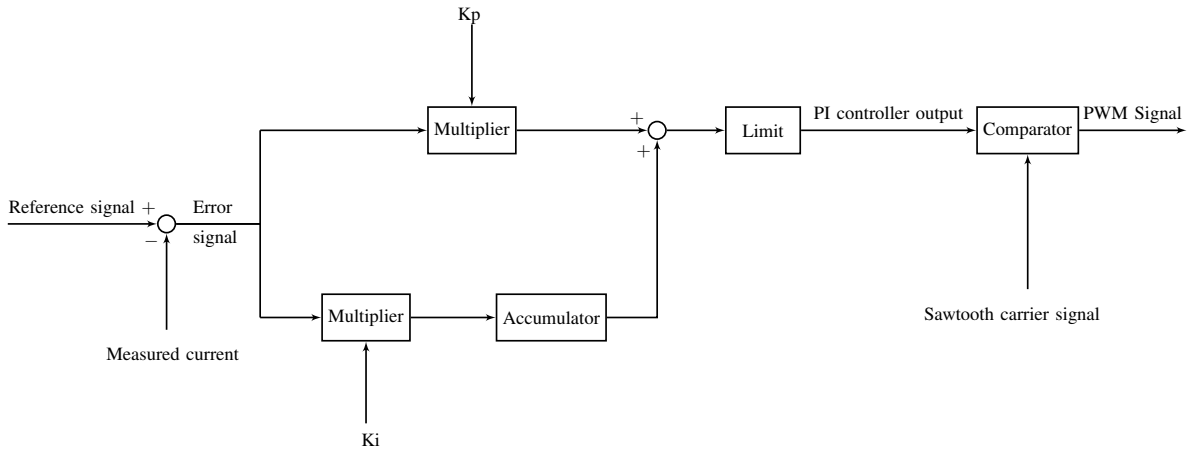

Figure 3.11: Digital PI controller and pulse width modulator

At every stage in the current regulation process, the data width varies from stage to stage. At the summing stage, the data bit width increases by one bit. Moreover at the output of every multiplier block, the output width is the sum of the width of its input signals. However the varying bit widths, risks truncation of signals that will lead to rounding off errors. In order to solve this problem, a fixed point package, *fixed_generic_pkg.vhdl* is used in VHDL. The package is designed to avoid any possibility of bits overflow. The conventional packages, *numeric_std*, throws away underflow and overflow bits. Furthermore, the fixed point package is used to represent numbers that are less than 1.0 and also negative values using the *sfixed* data type. A width is assigned to a fixed point number and an assigned location of the decimal point. Moreover, the package has a function called *resize* function that can be used to ensure that the fixed point number has a sufficient bit width. The package has the advantage of being almost as fast as the conventional *numeric_std* arithmetic library.

The output of the proportional gain stage and the integral stage are summed together and passed through a limiter as shown in Figure 3.11. The limiter ensures that the signal stays within the operating range of the pulse-width modulator i.e. the signal should be between zero and one. At the modulation stage, the PI controller output signal is compared with the sawtooth carrier signal using the comparator algorithm. The comparator algorithm ensures that there are no multiple crossings between the PI controller output signal and the sawtooth carrier signal. After the comparator algorithm compares the PI controller output and the sawtooth carrier signal, a PWM signal is generated. The algorithm to generate the sawtooth carrier signal is discussed in the following section and also the technique employed by the comparator to generate PWM signals.

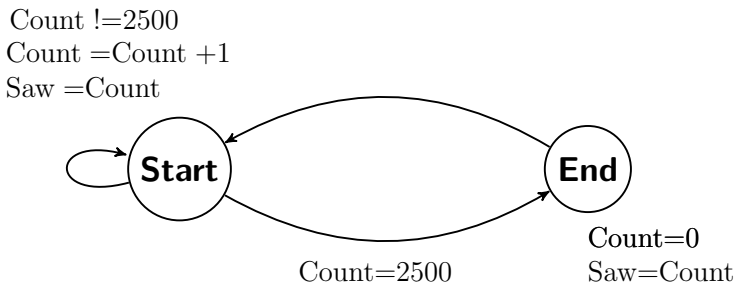

Figure 3.12: Sawtooth generation finite state machine

3.2.5 Sawtooth and PWM generation technique

According to the small-signal model used for control loops design and discussed in Chapter 5, a series of impulses are generated by the sampling comparator at every crossing between the carrier signal and the PI controller output signal. In the case of a sawtooth carrier signal, the impulses generated are spaced equidistantly from each other in time with a sampling period equal to the switching period T_s. For this reason, the sawtooth carrier signal is considered in this project for pulse width modulation. In order to create a sawtooth signal that generates impulses with a sampling period of T_s, a counter is created with a maximum value calculated using Equation 3.2.4.

$$\begin{aligned} Counter &= \frac{Clock}{Switching\ frequency} \\ &= \frac{50\,\text{MHz}}{20\,\text{kHz}} \\ &= 2500 \end{aligned} \tag{3.2.4}$$

The sawtooth generation process is shown by the finite state machine in Figure 3.12. For every clock cycle, the counter increments by one until it reaches its maximum of 2500 and resets to zero. The time taken for the counter to count from zero to 2500 is 50 µs which is the switching period as shown in Figure 3.13. As the input signal into the the pulse width modulator crosses the sawtooth carrier signal, a PWM output signal is generated, as shown in Figure 3.13.

3.2.6 Blanking time

The synchronous DC/DC buck converter implements two switches namely S_1 and S_2. The switches are complementary implying that when switch S_1 is on, S_2 should be off and vice versa. The switches S_1 and S_2 are controlled by the gate signals $PWMH$ and $PWML$, respectively. The IGBT module used by the DC/DC converter never goes from the ON state to the OFF or vice versa instantaneously because each switch in the module

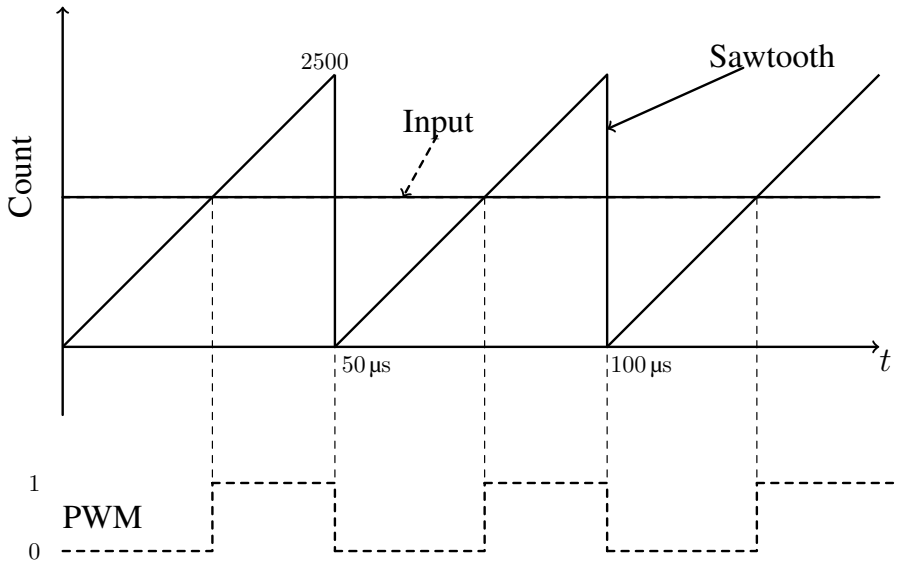

Figure 3.13: Pulse width modulation technique

has a gate charge and a discharge time. However a blanking/dead time, a period where both switches are turned off, is included in the gate signals. The dead time between $PWMH$ and $PWML$ ensures that S_1 completely turns off before S_2 is turned on and vice versa. The dead time period ensures that the converter does not experience a shoot through problem. The more dead time there is, the output voltage is slightly reduced and the shorter is it the greater the chances of experiencing shoot through problem. Therefore careful fine tuning of the dead time is carried out in order to ensure the balance between slight reduction in output voltage and the risk of experiencing a shoot through problem.

The finite state machine in Figure 3.14 is designed to create a dead time between $PWMH$ and $PWML$ signals. The state *Modulation* is the pulse width modulator described in the previous section and it creates two complementary signals namely, PWM and $\overline{PWM}$. The signals are 180° out of phase but without a blanking/dead time between them. The state *Blanking* checks whether PWM or $\overline{PWM}$ are either in a logic state of zero or one. A delay counter is created that increments by one at every clock cycle up to a maximum value of 25. When the counter reaches 25, it corresponds to a time delay of 500 ns which is the dead time being designed for. The dead time is carefully chosen in order to avoid a shoot through problem and also ensuring correct operation of the converter. If the PWM signal is in a logic state of one, the delay counter *D1* is triggered. A delay of 500 ns is imposed on the PWM signal before it is assigned to the $PWMH$ signal. Moreover if the PWM has a logic state of zero, no delay is imposed and the signal is assigned to $PWMH$. The $PWMH$ becomes the gate signal that drives the S_1

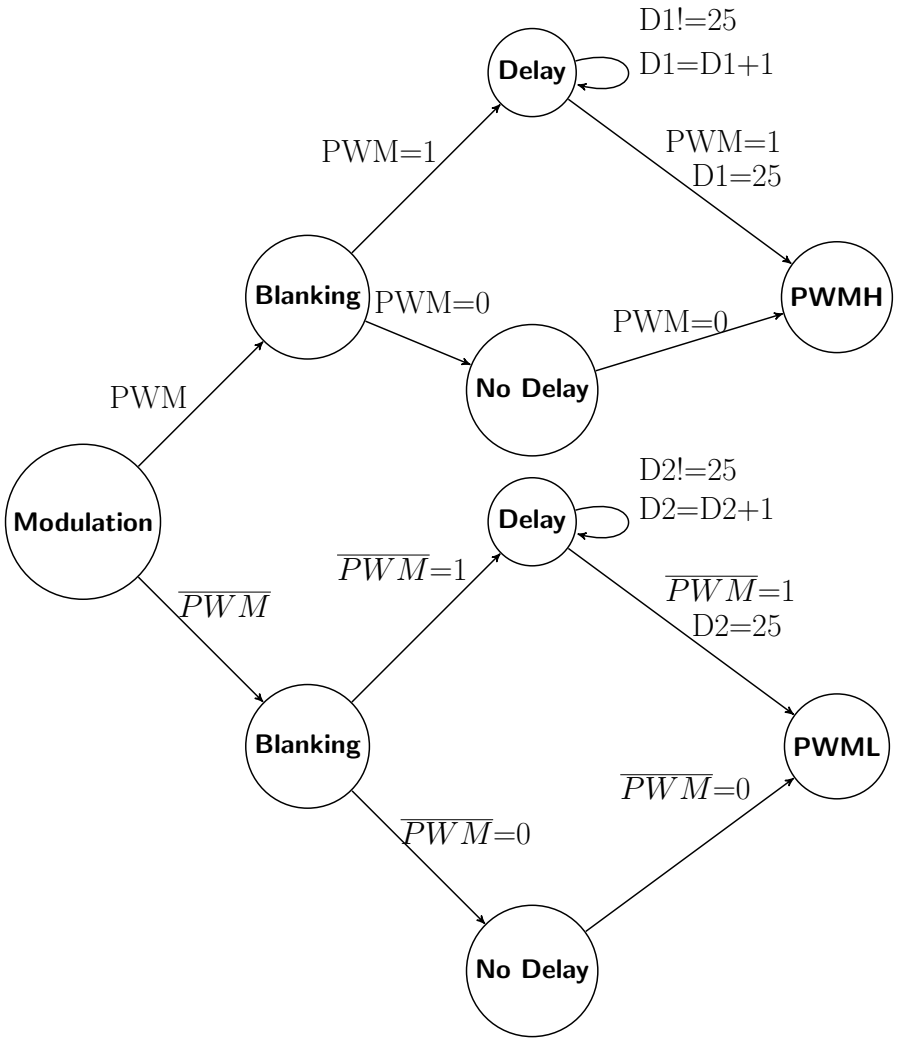

Figure 3.14: Blanking time generation state machine

switch. Furthermore, if the $\overline{PWM}$ signal has a logic state of one, it is delayed for 500 ns before it is assigned to the $PWML$ signal. If the $\overline{PWM}$ signal has a logic state of zero, no delay is imposed on the signal and it is assigned to the $PWML$ signal. The $PWML$ signal becomes the lower side switch, S_2 gate signal. Therefore the signals $PWMH$ and $PWML$ are complementary signals with a blanking time of 500 ns. The generated $PWMH$ and $PWML$ signals are shown in Figure 3.15.

3.3 Summary

In this chapter the functions of the SAE system are discussed. The SAE system is designed to operate in two modes namely the simulation and the emulation mode. Both modes of operation are illustrated in greater detail. Different software algorithms implemented

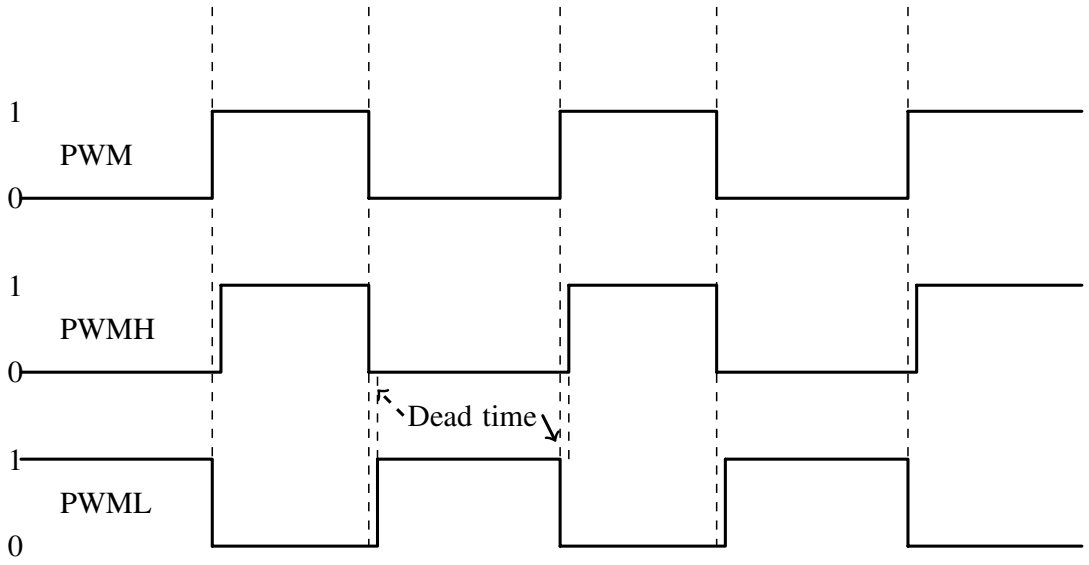

Figure 3.15: Pulse width modulation with blanking time

by the system responsible for UART serial communication, A/D converter, pulse width modulation and current control regulation are discussed. The A/D converter if tested for accuracy in taking measurements and random spikes are observed. Several measures were taken in order to eliminate the occurrence of spikes but to no avail. However it is concluded that the occurrence of such spikes is attributed to the non-ideal performance of the A/D converter and noise signals from the switching power supply circuits.

Chapter 4

Hardware design

The Solar Array Emulator (SAE) system with a block diagram shown in Figure 4.1, is composed of four sub-systems namely:

1. The Field Programmable Gate Array (FPGA) device.
2. The synchronous DC/DC buck converter.
3. The graphical user interface (GUI) running on the personal computer (PC).
4. The load characteristics under evaluation.

According to Figure 4.1, the algorithm running on the PC transmits a reference current to the FPGA board and in return, the FPGA transmits the load current and voltage measurements to the PC via serial communication port. The current control algorithm running in the FPGA device regulates the load current of the DC/DC converter using the pulse-width modulation (PWM) principle. The load connected to the DC/DC converter is the photovoltaic power electronic system under evaluation by the SAE system. The DC/DC converter bus voltage is generated by a DC power supply. However the design of the DC power supply is beyond the scope of this project. A much detailed description of the operation of the SAE system shown in Figure 4.1 is given in Chapter 3.

In this chapter the design and development of the hardware systems implemented by the SAE system is presented. The hardware systems include the synchronous DC/DC

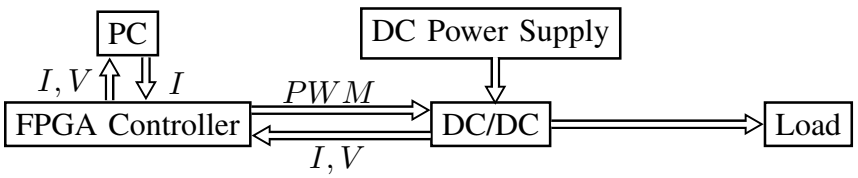

Figure 4.1: Solar Array Emulator block diagram

converter, the current and voltage sensors, the gate driver circuitry and the isolated power supply. The DC/DC converter is responsible for the current regulation. The gate driver circuitry is implemented as medium to transmit the gate signals generated by the FPGA device to the DC/DC converter. Moreover, the isolated power supply is responsible for powering the gate driver circuit as well as the voltage and current measurement board. The detailed design strategies for these hardware systems are discussed in the following sections.

4.1 Synchronous Buck Converter Design

The DC/DC converter is used by the SAE system for regulation of current and voltage based on the PWM principle. The DC/DC converter specifications, waveforms and components design are described in the following sub-sections.

4.1.1 Converter Specifications and waveforms

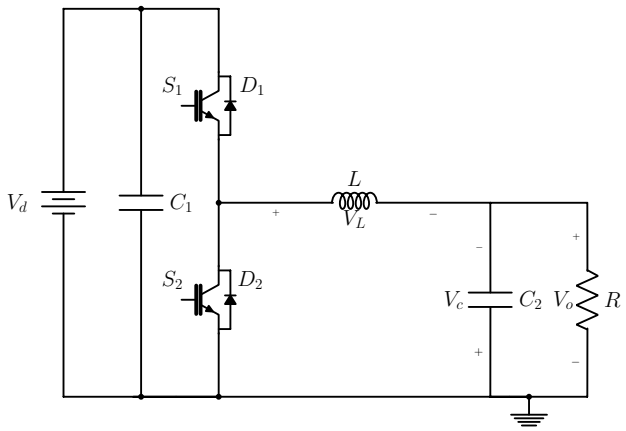

Figure 4.2: Synchronous buck converter

Table 4.1: Converter parameters

DC-bus voltage (V_d)	900 V
Maximum output current $I_{o(max)}$	18 A
Switching frequency (f_s)	20 kHz
IGBT specifications	
On-state voltage ($V_{on(IGBT)}$)	2.7 V
Turn-on time ($t_{C(on)}$)	135 ns
Turn-off time ($t_{C(off)}$)	450 ns
Diode on voltage ($V_{on(Diode)}$)	2.9 V

The converter shown in Figure 4.2 is rated at 20 kW and designed using the system parameters in Table 4.1. The synchronous buck converter is designed for maximum ripple current. The ripple current Δi_L of the converter shown in Figure 4.3 is designed to be in the range of 20% to 40% of the maximum inductor current $I_{o(max)}$ as illustrated by Equation 4.1.1, and is valued at 5.4 A.

$$\Delta i_L = 30\% I_{o(max)} \tag{4.1.1}$$

The relationship between the input and the output voltage is illustrated by Equation 4.1.2 where D, is the duty cycle.

$$V_o = DV_d \tag{4.1.2}$$

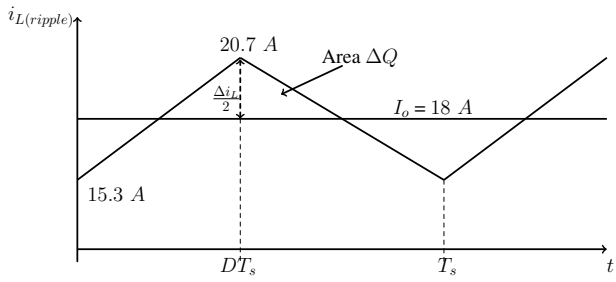

Figure 4.3: Current through the inductor

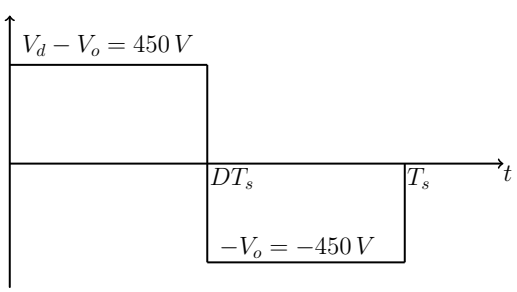

Figure 4.4: Voltage across the inductor

The ripple current Δi_L is determined using the Equation 4.1.3 where L is the inductance, based on Figure 4.3.

$$\Delta i_L = \frac{V_d(1-D)D}{Lf_s} \tag{4.1.3}$$

In order to determine the value of D for which the peak to peak ripple current will be maximum, the derivative of the ripple current as a function of D is determined using Equation 4.1.4.

$$\frac{d\Delta i_L}{dD} = (1-2D) = 0 \tag{4.1.4}$$

The duty cycle is calculated as 0.5 at maximum peak-peak ripple current. Thus the waveforms are drawn at a duty cycle of 0.5. When switch S_1 is turned on, the inductor current i_L does not change instantaneously and it increases from $i_{L(min)}$ to $i_{L(max)}$ in 25 µs (DT_s). When the switch S_1 is turned off, the inductor current reduces from $i_{L(max)}$ to $i_{L(min)}$, as shown in Figure 4.3. Moreover, during conduction of S_1, the voltage across the inductor v_L is the voltage difference between the source voltage V_d and the output voltage V_o. As previously mentioned, V_d is generated by a separate DC power supply which is not covered in this project. However, when switch of S_1 is turned off, the voltage across the inductor is equivalent to the voltage across the filter capacitor. Figure 4.4 shows the voltage across the inductor per switching period. Switch S_2 does not conduct as current is only flowing from the source to the load and therefore S_1 and diode D_2 only conduct. When switch S_1 is conducting, the current through the switch i_{S1} is equivalent to i_L. However when S_1 is switched off, i_{S1} becomes zero as current no longer flows through the switch. The current i_{S1} waveform is shown in Figure 4.5. When S_1 is turned on, there is no voltage drop across the switch. Furthermore, when the switch is turned off, the voltage across the switch v_{S1} is equivalent to the source voltage V_d, as shown in Figure 4.6. Moreover, as S_1 is turned on, diode D_2 is reverse biased and as S_1 is turned off, D_2 is forward biased with a current i_{D2} equivalent to i_L, as shown in Figure 4.7. The voltage waveform for D_2 is shown in Figure 4.7. The synchronous buck converter is also

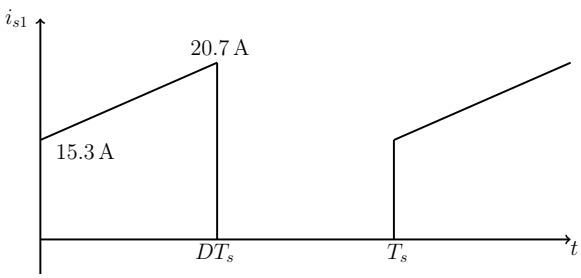

Figure 4.5: Current through the switch S_1

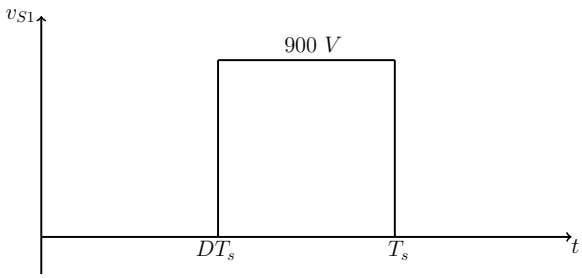

Figure 4.6: Voltage across the switch S_1

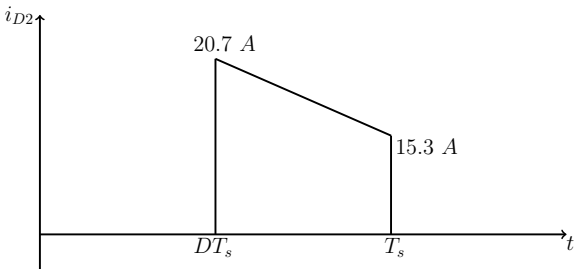

Figure 4.7: Current through the diode D_2

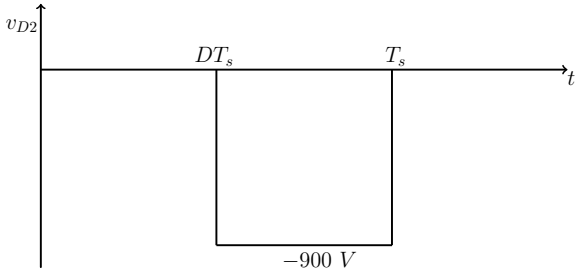

Figure 4.8: Voltage across the diode D_2

simulated and the waveforms in Appendix C are obtained. The simulation waveforms in Appendix C verifies the waveforms described above.

The two switches namely, S_1 and S_2 are switched using a complementary switching strategy and therefore if S_1 is on then S_2 will be off. The phenomenon of discontinuous current will not occur in the synchronous DC/DC converter because the S_2 and the diode D_1 will provide the path for the negative inductor current. However, the converter is designed to operate at high currents so an assumption is made that the current does not ever become.

4.1.2 Designing the filter inductor for maximum current ripple

The inductor is designed for the maximum output current at a duty cycle of 0.5. Therefore the value of a duty cycle of 0.5 is used to derive the equation for the maximum peak to peak ripple and illustrated in Equation 4.1.5.

$$\Delta i_{L(max)} = \frac{V_d(1-0.5)0.5}{Lf_s}$$

$$\Delta i_{L(max)} = \frac{V_d}{4Lf_s} \tag{4.1.5}$$

By re-arranging Equation 4.1.5, the expression for calculating inductance is illustrated by Equation 4.1.6. Using the derived expression for inductance, the value of inductance

is calculated as 2.08 mH.

$$\begin{aligned} L &= \frac{V_d}{4 f_s \Delta i_{L(max)}} \\ &= \frac{900}{4(5.4)(20 \times 10^3)} \\ &= 2.08\,\text{mH} \end{aligned} \tag{4.1.6}$$

4.1.3 Designing the output filter capacitor

In order to determine the filter capacitance, the area ΔQ in Figure 4.3, equivalent to the accumulated charge, is determined using Equation 4.1.7. The accumulated charge is calculated using the equation $Q = \int_0^t i_L t\, dt$ and this is achieved by taking the area of ΔQ in Figure 4.3.

$$\begin{aligned} \Delta Q &= \left(\frac{1}{2}\right)\left(\frac{T_s}{2}\right)\left(\frac{\Delta i_L}{2}\right) \\ &= \frac{T_s \Delta i_L}{8} \end{aligned} \tag{4.1.7}$$

The formula to calculate the accumulated charge ΔQ, is $\Delta Q = \Delta V_o C_2$. By designing for a maximum ripple voltage $\Delta V_{o(max)}$ of 2.5 V, Equation 4.1.8, derived from Equation 4.1.7 is used.

$$\Delta V_{o(max)} = \frac{T_s \Delta i_{L(max)}}{8 C_2} \tag{4.1.8}$$

By re-arranging Equation 4.1.8, the output filter capacitance is determined using Equation 4.1.9 as follows.

$$\begin{aligned} C_2 &= \frac{\Delta i_{L(max)}}{8 f_s \Delta V_{o(max)}} \\ &= \frac{5.4}{8(20 \times 10^6)2.5} \\ &= 13.5\,\mu\text{F} \end{aligned} \tag{4.1.9}$$

4.1.4 Designing the input bus capacitor

The objective of designing the bus capacitors is to reduce the ripple voltage amplitude seen at the input of the converter. The bus capacitor is connected to the separate DC power supply that generates a DC bus voltage. If the DC power supply is an infinitely stiff voltage source, it can regulate the voltage perfectly. Therefore no current will flow through the bus capacitor because there will be no change in voltage across the capacitor. However, for the design of the input bus capacitor for this project, a worst case assumption of the DC power supply is made. It is assumed that the DC power supply has a very

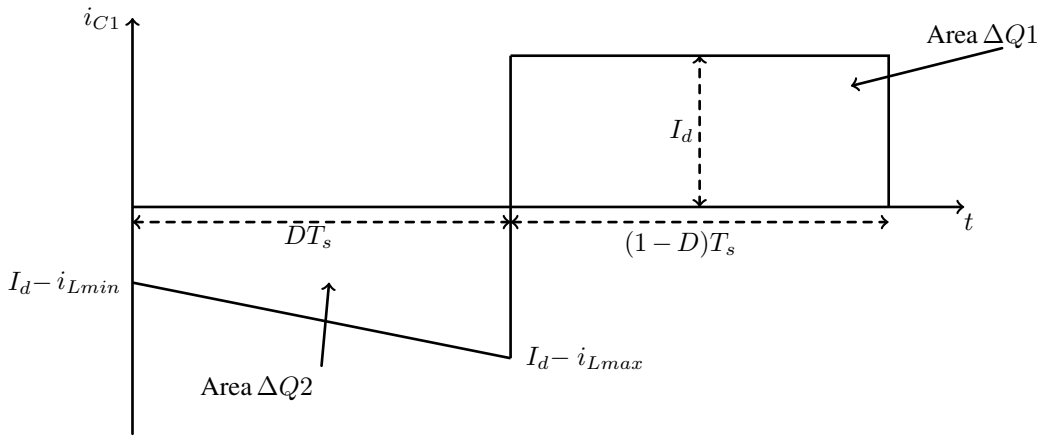

Figure 4.9: Current through the bus capacitor

high output impedance at the synchronous buck converter's switching frequency. The maximum input ripple current amplitude occurs at the maximum output load current. The waveform for current through the bus capacitor is shown in Figure 4.9. The single phase bi-directional converter reaches its maximum ripple current at 50% duty cycle.

The bus capacitor is designed for maximum peak to peak ripple current at 50% duty cycle. Figure 4.10 verifies that the bus capacitance should be designed at 50% duty cycle where the ripple current is maximum. The areas $\Delta Q1$ and $\Delta Q2$ in Figure 4.9, represent the accumulated charge in the capacitor and are described by Equation 4.1.10 and Equation 4.1.11, respectively.

$$\Delta Q1 = I_d(1-D)T_s \tag{4.1.10}$$

$$\Delta Q2 = 0.5DT_s(i_{L(max)} + i_{L(min)} - 2I_d) \tag{4.1.11}$$

But $I_d = DI_o$ and $C = \frac{\Delta Q}{\Delta V_c}$. Therefore by using area $\Delta Q1$, the bus capacitance is determined using Equation 4.1.12.

$$\begin{aligned} C_1 &= \frac{I_o D(1-D)}{f_s \Delta V_c} \\ &= \frac{18(0.5^2)}{(20\times 10^3)2.5} \\ &= 90\,\mu\text{F} \end{aligned} \tag{4.1.12}$$

4.1.5 Inductor construction

The inductor is designed by taking into account different critical factors that ensure the inductor's core is not saturated at peak currents. Moreover, the designed inductor should

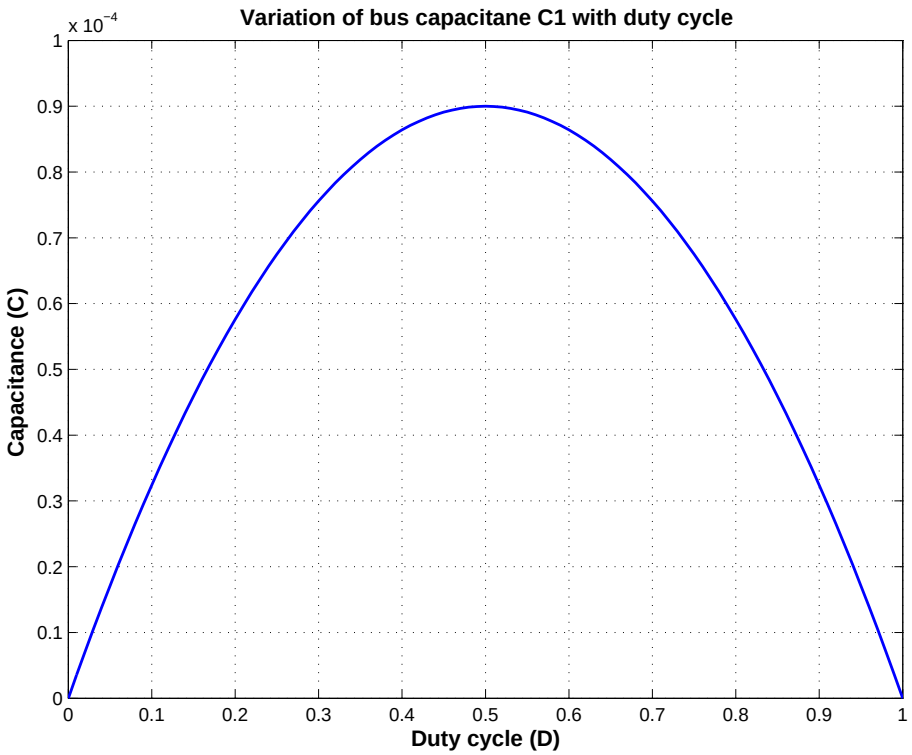

Figure 4.10: Design of bus capacitance with duty cycle at maximum ripple current

achieve the required inductance and be able to conduct maximum load current with minimum winding resistance and copper losses.

Different magnetic cores are used for inductor construction depending on the design specifications. The peak flux density in magnetic materials is limited by saturation and thermal constraints. The saturation limit poses a magnetic path constraint as current is increased [24]. The magnetic path constraint is illustrated by Equation 4.1.13 where L is the inductance, I_m is the peak current, Φ_m is the maximum flux, B_m is the maximum flux density, A_c is the cross sectional area of the magnetic core used and N is the number of turns in the window area.

$$LI_m = N\Phi_m = NB_mA_c \tag{4.1.13}$$

A thermal limit is experienced when a maximum current carrying capacity of the conductor is exceeded and the conductor generates heat. The generated heat damages the insulation on the conductor and melts the conductor. The heat is generated according to the Equation 4.1.14 where Q is the generated heat, I is the current flowing, R is the conductor resistance and t is the time taken during conduction.

$$Q = I^2Rt \tag{4.1.14}$$

The thermal constraint is illustrated using Equation 4.1.15, where K_w is the window utilisation factor, J is the copper wire current density and A_w is the area of copper path.

Thick Litz wire with properties shown in Table 4.2 is used for conduction in order to reduce the skin effect and proximity effect losses when conducting at high frequencies [25].

$$NI_{rms} = K_w A_w J \tag{4.1.15}$$

The product of Equation 4.1.13 and Equation 4.1.15 is the energy equation for the inductor design. The energy equation in Equation 4.1.16 entails that the inductor design specifications on the left hand side of the equation should equal the product of the area of the magnetic path A_c and the area of the copper path A_w on the right hand side.

$$\frac{LI_m I_{rms}}{K_w B_m J} = A_c A_w \tag{4.1.16}$$

Table 4.2: Inductor design specifications

Inductance (L)	2.08 mH
Maximum current(I_m)	20.7 A
Current density J	3 A mm^{-2}
Maximum flux density B_m	0.25 T
Winding factor K_w	0.5
Litz wire AWG [number of strands]	34[60]

Table 4.3: Core specifications

Core type, shape and size	EE/65/32/27
Cross sectional area A_c	1070 mm^2
Winding area (A_w)	540 mm^2

The maximum inductor current is calculated as $I_m = I_{o(max)} + \frac{1}{2}\Delta i_{L(max)}$. Using Equation 4.1.16 the energy product is calculated as follows:

$$\begin{aligned}\frac{LI_m I_{rms}}{K_w B_m J} &= \frac{(2.08 \times 10^{-3})(20.7^2)}{(0.5)(0.25)(3 \times 10^6)} \\ &= 2.37 \times 10^{-6}\,\text{m}^4 \\ &= 2.37 \times 10^{6}\,\text{mm}^4\end{aligned}$$

The product of the actual values of A_c and A_w shown in Table 4.3, is calculated as 577.80 mm^4. As previously mentioned, the energy equation in Equation 4.1.16 is satisfied if the right hand side is equal to the left hand side. In order for the product of the actual values of A_c and A_w in Table 4.3 to satisfy Equation 4.1.16, the number of cores required using EE/65/32/27 ferrite cores is calculated as:

$$\begin{aligned} N_i &= \frac{2.37 \times 10^6\,\text{mm}^4}{577.80 \times 10^3\,\text{mm}^4} \\ &\simeq 4 \end{aligned}$$

Therefore approximately four cores using EE/65/32/27 ferrite cores are required. The four cores will build four inductors that will be connected in series so that the product of A_c and A_w can satisfy Equation 4.1.16. Since the four inductors will be connected in series, each individual inductor has an inductance of 0.52 mH obtained from dividing the calculated total inductance of 2.08 mH by four. The calculation is based on the fact that the total inductance of inductors in series is the summation of the individual inductances. The number of turns in each inductor are calculated using Equation 4.1.17.

$$\begin{aligned} N &= \frac{LI_m}{B_m A_c} \\ &= \frac{(0.52 \times 10^{-3})(20.7)}{0.25(1070 \times 10^{-6})} \\ &\simeq 40 \end{aligned} \tag{4.1.17}$$

The air gap length L_g is calculated in each core is calculated using Equation 4.1.18.

$$\begin{aligned} L_g &= \frac{N^2 A_c \mu}{L} \\ &= \frac{40^2(1070 \times 10^{-6})(4\pi \times 10^{-7})}{0.52 \times 10^{-3}} \\ &= 0.004\,137\,\text{m} \end{aligned} \tag{4.1.18}$$

Therefore the air gap length at the extreme end of each core is 2 mm. The actual winding losses are determined using Equation 4.1.19.

$$\begin{aligned} P &= I_m^2 R \\ &= (20.7^2)0.5 \\ &= 214.245\,\text{W} \end{aligned} \tag{4.1.19}$$

4.2 IGBT power losses

Careful consideration is taken in selecting the IGBT module suitable for the SAE system's dynamic performance. The IGBT module used for the DC/DC converter in Figure 4.2 is a FF50R12RT4 module from Infineon. The IGBT specifications are illustrated in Table 4.1. Moreover, the IGBT switch has a maximum collector-emitter voltage V_{CES} of 1200 V and a maximum continuous DC collector current I_C of 50 A. As previously discussed, only

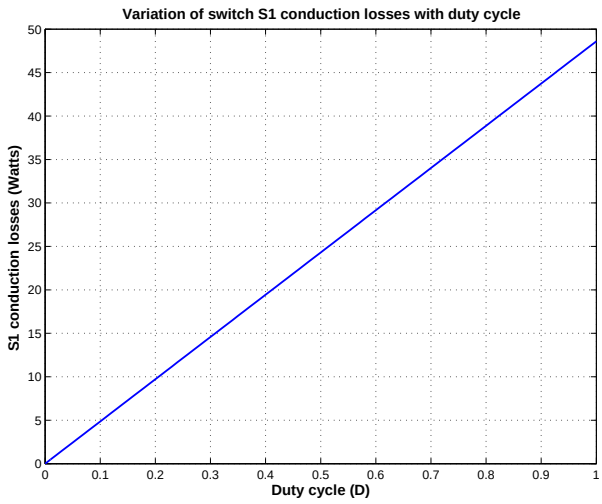

Figure 4.11: Switch S_1 conduction losses

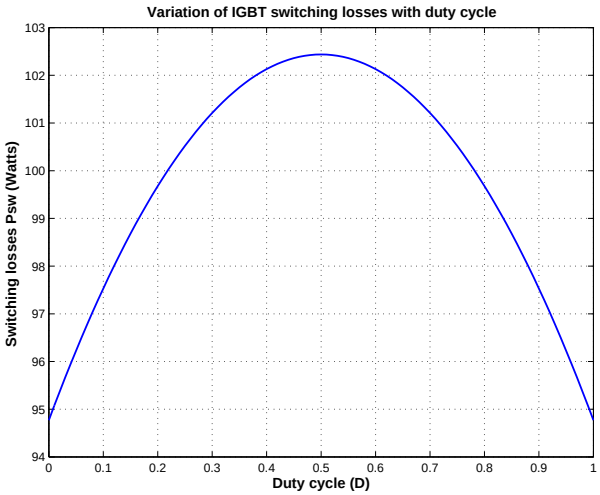

Figure 4.12: Switch S_1 switching losses

the switch S_1 and the diode D_2 conduct and the current i_{S1} and current i_{D2} are shown in Figure 4.5 and Figure 4.7, respectively. Switch S_2 is turned on but does not conduct and neither does the diode D_1 as previously discussed. It is observed in the i_{S1} and i_{D2} current waveforms that the duration per switching cycle for either the diode or the switch to conduct depends on the duty cycle D and therefore the power losses are also dependent on D.

4.2.1 S1 switching and conduction losses

The IGBT switching losses are calculated using Equation 4.2.1 used in [26] where $i_{L(min)}$ and $i_{L(max)}$ are minimum and maximum inductor current, respectively. The IGBT turn on $t_{d(on)}$ and turn off $t_{d(off)}$ times are defined in Table 4.1.

$$P_{switch(IGBT)} = \frac{1}{2} V_d f_s \left(i_{L(min)} t_{d(on)} + i_{L(max)} t_{d(off)} \right) \tag{4.2.1}$$

The conduction losses of the IGBT are calculated using Equation 4.2.2.

$$\begin{aligned} P_{cond(IGBT)} &= \frac{V_{on(IGBT)}}{T_s} \int_0^{T_s} i_{S1} dt \\ &= \frac{V_{on(IGBT)}}{T_s} \left(\left(I_o - \frac{\Delta I_L}{2} \right) D T_s + \frac{D T_s \Delta I_L}{2} \right) \\ &= V_{on(IGBT)} \left(i_{L(min)} D + \frac{D}{2} \Delta I_L \right) \end{aligned} \tag{4.2.2}$$

The variations of the conduction and the switching power losses with the duty cycle are shown in Figure 4.11 and Figure 4.12, respectively. The total of the switching and the conduction losses is represented in Figure 4.13. The maximum power loss is realised at the duty cycle of one and valued at 143.37 W.

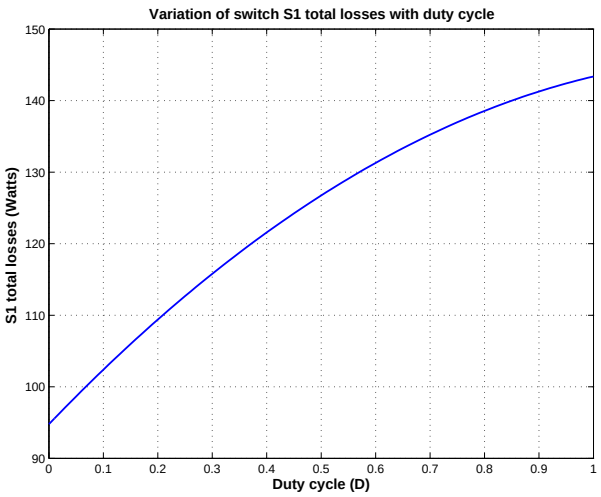

Figure 4.13: Switch S_1 total power losses

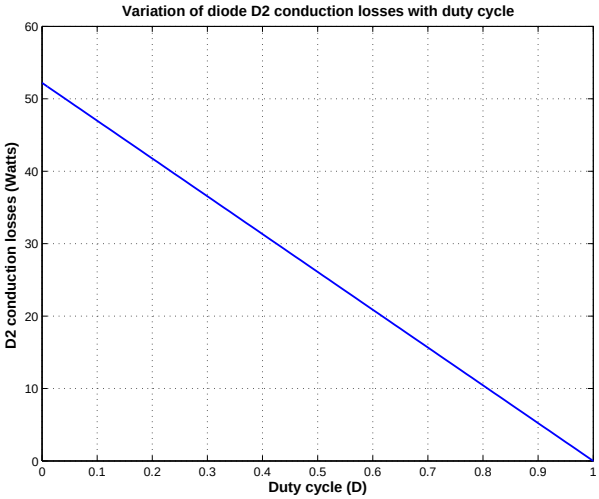

Figure 4.14: Diode D_2 conduction losses

4.2.2 D2 conduction losses

The diode D_2 conduction losses are calculated using the expression in Equation 4.2.3. The equations are derived from the waveform in Figure 4.7.

$$\begin{aligned} P_{cond(diode)} &= \frac{V_{on(Diode)}}{T_s}\int_0^{T_s} i_{D2}dt \\ &= \frac{V_{on(Diode)}}{T_s}\left(i_{L(min)}T_s(1-D)+\frac{T_s\Delta I_L}{2}(1-D)\right) \\ &= V_{on(Diode)}\left(i_{L(min)}(1-D)+\frac{1-D}{2}\Delta I_L\right) \end{aligned} \tag{4.2.3}$$

The variation of the diode D_2 conduction losses with the duty cycle are shown in Figure 4.14. The maximum power of 52.2 W is lost at the duty cycle of zero.

4.3 Heat sink Design

A heat sink is required to absorb and disperse heat away from the IGBT module. The thermal resistance, $\theta_{(s-a)M}$ is the one parameter that changes dynamically depending on the airflow available [27]. The thermal resistance determines the characteristics of a heat sink suitable for use in dispersing heat away from the IGBT module. Figure 4.15 shows the heat-sink design block diagram representation. The specifications for determining the suitable heat sink are given in Table 4.4. The formula to calculate the junction temperature is given by Equation 4.3.1 as derived from the block diagram in Figure 4.15.

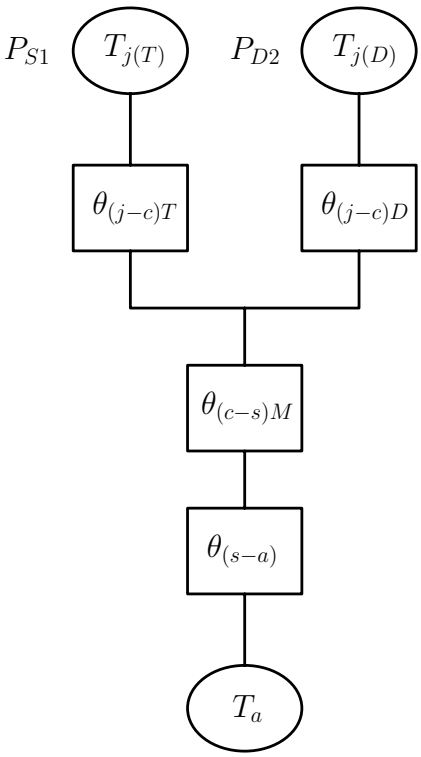

Figure 4.15: Heat-sink design representation

Table 4.4: Heat sink specifications

Diode D_2 power loss (P_{D2})	52.2 W
Switch S_1 power loss (P_{S1})	143.37 W
IGBT junction-case ($\theta_{(j-c)T}$)	0.3 °C W^{-1}
Diode junction-case ($\theta_{(j-c)D}$)	0.6 °C W^{-1}
Module case-sink ($\theta_{(c-s)M}$)	0.05 °C W^{-1}
Maximum junction temperature ($T_{j(T)}$)	150 °C
Ambient temperature (T_a)	40 °C

$$T_{j(T)} = P_{S1}\theta_{(j-c)T} + [(P_{S1} + P_{D2})\theta_{(c-s)M}] + [(P_{S1} + P_{D2})\theta_{(s-a)M}] + T_a \tag{4.3.1}$$

By re-arranging Equation 4.3.1, the sink-ambient thermal resistance $\theta_{(s-a)M}$ of the module is calculated using the expression in Equation 4.3.2.

$$\begin{aligned}\theta_{(s-a)M} &= \frac{T_{j(T)} - T_a - (P_{S1}\theta_{(j-c)T}) - [(P_{S1} + P_{D2})\theta_{(c-s)M}]}{P_{D2} + P_{S1}} \\ &= \frac{150 - 25 - (143.37 \times 0.3) - ((143.37 + 52.2)0.05)}{143.37 + 52.2} \\ &= 0.3694\,\text{°C W}^{-1}\end{aligned} \tag{4.3.2}$$

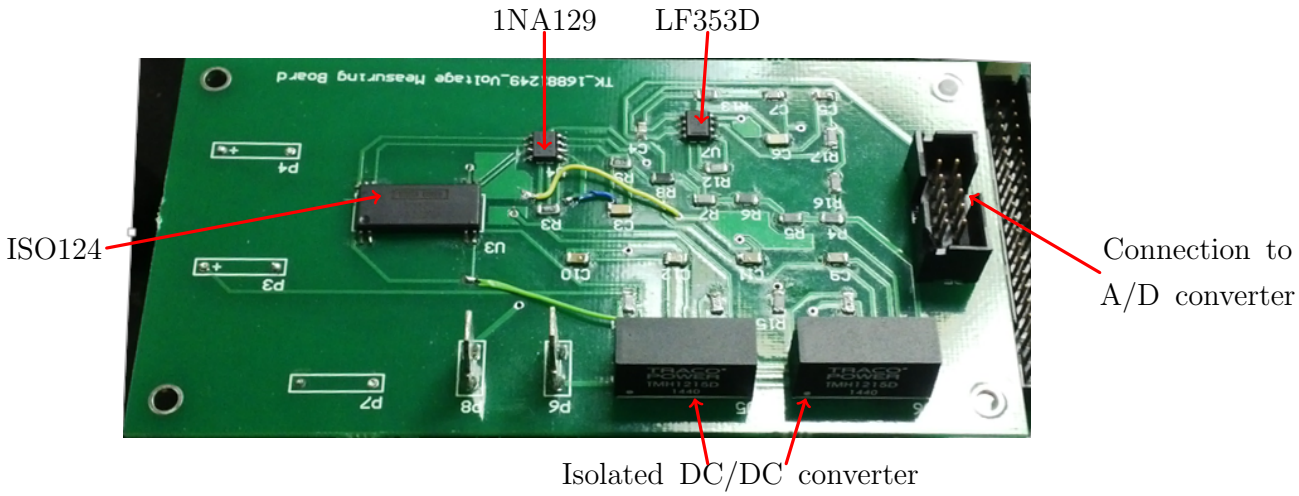

Figure 4.16: Voltage Sensing Board

The heat sink selected for dispersing heat away from the IGBT has a thermal resistance lower than $0.3694\,^{\circ}\mathrm{C\,W^{-1}}$, which qualifies it as the suitable heat sink.

4.4 Voltage Sensor Design

The voltage sensor is required to measure the DC/DC converter's output voltage. The voltage sensor is made up of a potential divider resistive network connected to a series of low power amplifier and filtering circuits. The resistive potential divider network scales down the voltage to be measured and its output is buffered by a differential amplifier, 1NA129 chip. The differential amplifier is responsible for amplification of weak signals and its output is connected to an isolation amplifier, ISO124 chip. The isolation amplifier is responsible for isolating the low voltage A/D converter side from the high voltage DC/DC converter side. The output of the isolation amplifier is connected to a dual operational amplifier, LM353 chip. Any noise that might still be part the voltage signal after amplification and isolation is filtered out by the operational amplifier. The voltage sensing printed circuit board (PCB) is shown in Figure 4.16. The chips used i.e. 1NA129, ISO124 and the LM353 integrated circuits and their corresponding component values are described in the following sections.

4.4.1 INA129

The INA129 chip is a general purpose, high precision and low power instrumentation amplifier. The instrumentation amplifier is used to amplify the weak output signal of the potential divider network. The differential amplifier has a high input impedance

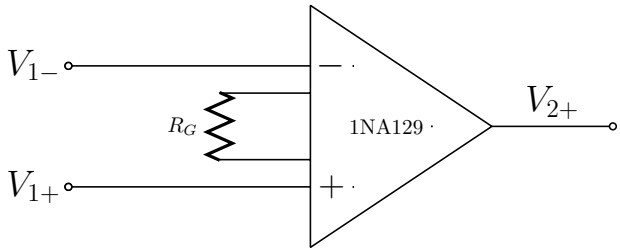

Figure 4.17: Simple block diagram of 1NA129 instrumentation amplifier

and a low output impedance, which qualifies it for amplification of a weak signal. The amplifier is characterised by high open loop gain, low noise, high common-mode rejection ratio (CMRR) and very low DC offset. The block diagram of the differential amplifier is shown in Figure 4.17. The input to the amplifier, V_{1+} and V_{1-} are the outputs of the potential divider resistive network. The gain of the amplifier is calculated using Equation 4.4.1.

$$G = 1 + \frac{49.4k\Omega}{R_G} \tag{4.4.1}$$

The resistor R_G is a single external resistor connected between pins 1 and 8 of INA129 integrated circuit for gain setting. To achieve a gain value of approximately two, a 49.9 kΩ resistor is used.

4.4.2 ISO124

The isolation amplifier is a galvanically isolated amplifier used to ensure electrical isolation between the low power FPGA side and the high power DC/DC converter side. Figure 4.18 shows the simple block diagram of the isolation amplifier. The isolation amplifier does not have any external components and has a continuous isolation voltage of 1500 V_{rms}. The input signal to the isolation amplifier, V_{2+}, is the output voltage signal of the 1NA129 instrumentation amplifier. The input signal is transmitted digitally across the differential capacitive barrier.

4.4.3 LM353

The dual operational amplifier is used as a Sallen-Key low-pass filter for filtering any noise after amplification and isolation. Two Sallen-Key 2nd order filter stages are cascaded together to form the large order filter shown in Figure 4.19. The input voltage signal V_{3+} to the filter network, is the output of the isolation amplifier. Each filter stage is designed individually in order to reduce complexity in transfer function derivation. The transfer

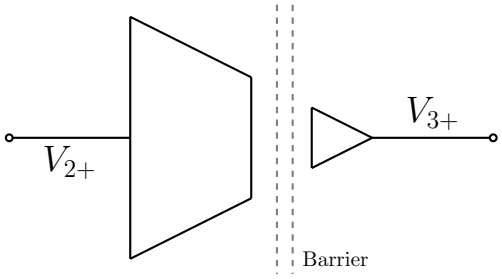

Figure 4.18: Simple block diagram of the ISO124 isolation amplifier

function in Equation 4.4.2 that describes the Sallen-Key opamp circuit in Figure 4.19 is derived using the following steps.

$$\begin{aligned} Vx &= i_{C2}R_2 + V_o \\ &= V_o R_2 C_2 s + V_o \\ &= V_o(R_2 C_2 s + 1) \end{aligned}$$

The sum of the currents at node V_x are calculated as follows:

$$i_{C2} = i_{C1} + i_{R1}$$

$$\frac{V_o}{1/sC_2} = \frac{V_{3+} - V_x}{R_1} + \frac{V_o - V_x}{1/sC1}$$

Substituting for V_x:

$$V_o(sR_1R_2C_1C_2 + s(R_1C_2s + 1) + sR_1C_1(R_2C_2s + 1) - sR_1C_1) = V_{3+}$$

After manipulating the above equation, a second order transfer function is obtained, as shown in Equation 4.4.2.

$$H(s) = \frac{1/R_1R_2C_1C_2}{s^2 + s(1/R_2C_1) + 1/R_1R_2C_1C_2} \tag{4.4.2}$$

The second order transfer function is of the form in Equation 4.4.3.

$$H(s) = \frac{\omega_o^2}{s^2 + s(\omega_o/Q) + \omega_o^2} \tag{4.4.3}$$

In order to calculate the capacitor and resistor values of each filter stage, the following equations are used. The following equations are obtained by equating the transfer function in Equation 4.4.2 to the second order transfer function form in Equation 4.4.3.

$$\omega_o^2 = \frac{1}{R_1R_2C_1C_2} \tag{4.4.4}$$

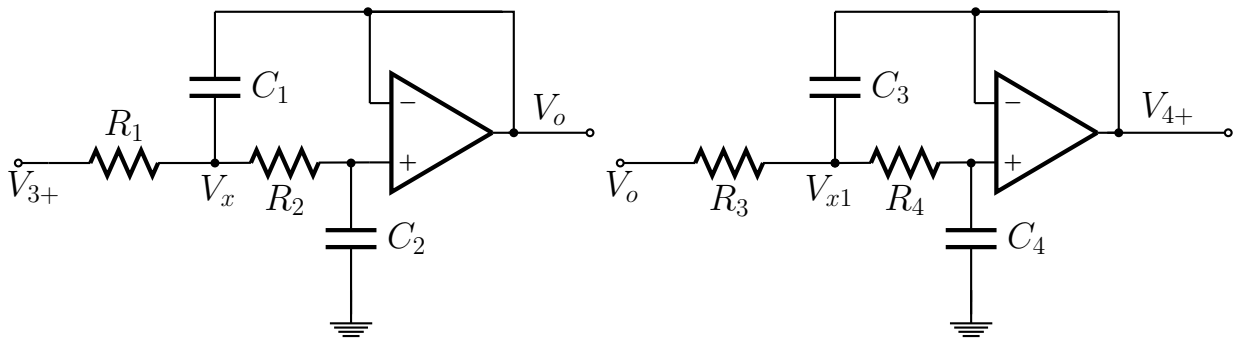

Figure 4.19: Sallen-Key filter stages

$$Q^2 = 0.5^2 \left(\frac{C_1}{C_2}\right) \tag{4.4.5}$$

Since there are many unknown parameters, it is decided to set R_1=R_2=R. The value of the resistance used for R_1 and R_2 is 10 kΩ. The designed value for the natural frequency f_o is 20 kHz and moreover, the value of the quality factor Q for the series cascade low-pass filters is 0.5. Equation 4.4.4 is simplified in Equation 4.4.6 to calculate the capacitor values.

$$\begin{aligned} C_1 &= \frac{1}{2\pi R f_o} \\ &= \frac{1}{2\pi(10\times10^3)(20\times10^3)} \\ &= 0.8\,\text{nF} \end{aligned} \tag{4.4.6}$$

Therefore the value of C_1 used is 1 nF. The Equation 4.4.5 is simplified to Equation 4.4.7 to calculate the value of C_2.

$$\begin{aligned} C_1 &= 4C_2Q^2 \\ &= 4C_20.5^2 \\ &= C_2 \end{aligned} \tag{4.4.7}$$

From Equation 4.4.7, it is observed that C_1 =C_2= 1 nF. The capacitors and resistors of the second filter stage i.e. C_3 , C_4 and R_3 , R_4, respectively are the same as the capacitor and resistor values of the first filter stage.

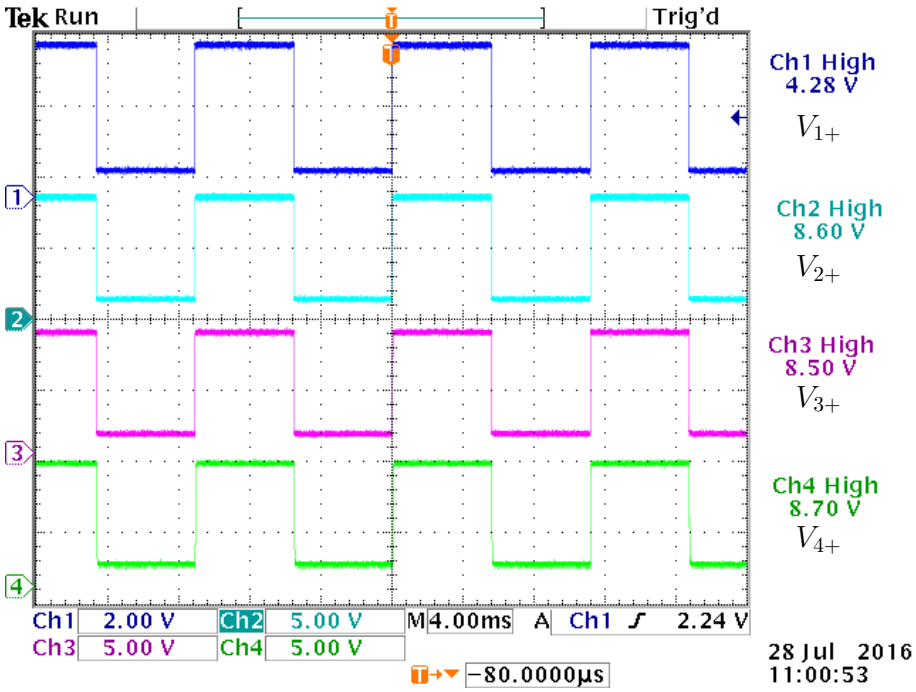

Figure 4.20: Voltage sensing measurements test

4.4.4 Voltage sensor test

The designed voltage sensor board is evaluated for performance in measuring voltage, as shown in Figure 4.20. The instrumentation amplifier, 1NA129, is given an input square wave voltage signal V_{1+} of 4.3 V. The amplifier is designed to have a gain of two and its output voltage signal V_{2+} measured 8.6 V and is the input voltage signal to the isolation amplifier. The output voltage of the isolation amplifier V_{3+} measured 8.50 V with approximately 1.17% deviation from the its input voltage. The output of the isolation amplifier V_{3+} is given as the input to the series cascaded Sallen-Key low-pass filter. The output of the low-pass filter V_{4+} measured 8.7 V with approximately 2.2% deviation from its input. Overall the voltage sensor board operates at approximately 98% accuracy and the deviation error is corrected in the algorithm running on the FPGA device.

4.5 Current Sensor Design

The current flowing through the inductor is measured using the LEM LTS 6-NP current transducer with block diagram shown in Figure 4.21. The current transducer implements galvanic isolation between the primary circuit (high power) and the secondary circuit (electronic circuit). The transducer employs the Hall effect principle for current measure-

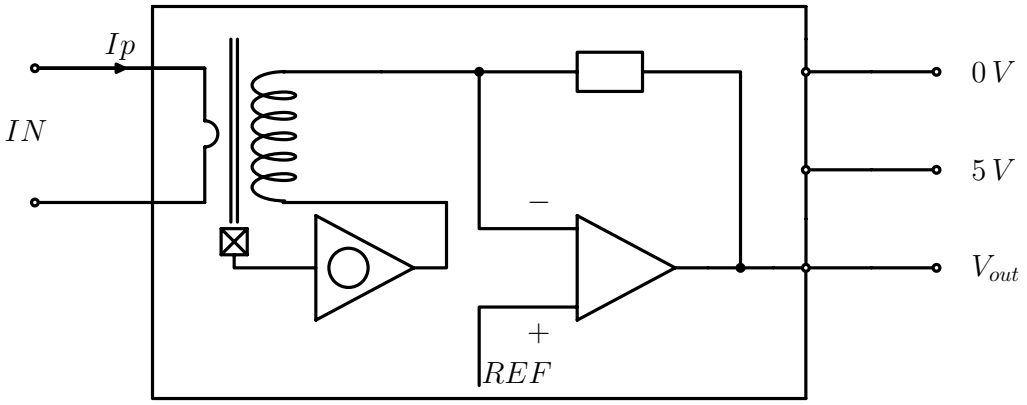

Figure 4.21: Current sensor Operation Principle

ments [28–30]. Moreover, it offers excellent accuracy, optimised response time, current overload capability and has a wide frequency bandwidth. The bandwidth is 100 kHz and the isolation voltage is 3 kV, tested for a period of one minute. The transducer is securely enclosed for high immunity to external interference. The output voltage V_{out}, shown in Figure 4.21 is calculated using the expression in Equation 4.5.1 where I_{PN} is the primary nominal current constant with a value of 6.

$$V_{out} = 2.5 + \frac{0.625 I_P}{I_{PN}} \tag{4.5.1}$$

The voltage generated V_{out} is read using the A/D converter on the FPGA device and the Equation 4.5.1 is re-arranged to Equation 4.5.2 in order to determine the actual value of the inductor current I_P being measured.

$$I_P = \frac{(V_{out} - 2.5) I_{PN}}{0.625} \tag{4.5.2}$$

4.6 Auxillary circuits

The main auxiliary circuit is the gate driver circuitry. The driver circuitry requires power and an isolated power supply is designed to cater for this. The design strategies of the gate driver circuitry and the isolated power supply are described below.

4.6.1 Gate driver circuitry

The gate driver circuit is employed as the medium to transmit generated gating signals from the FPGA device and the IGBT switches. The gate driver is essential because

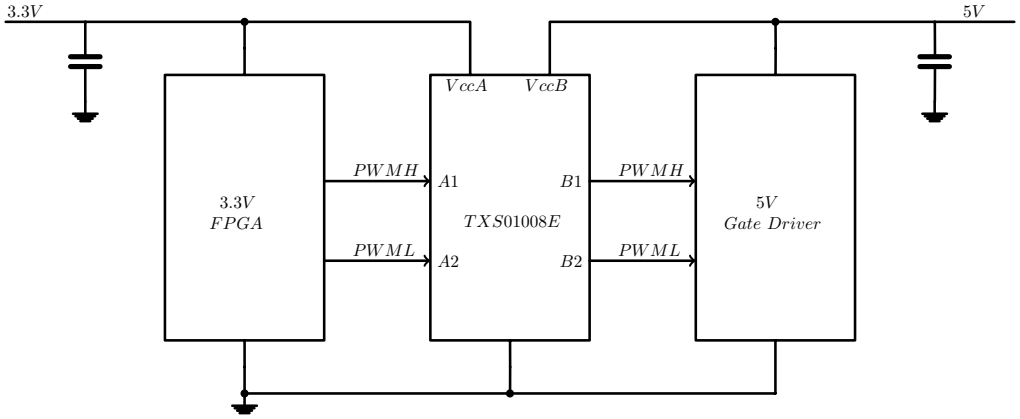

Figure 4.22: PWM Voltage translation

the generated PWM signals, 3.3 V level from the FPGA device, do not supply a high enough voltage, 15 V level, to physically switch on/off the IGBT switches. The issue of isolation between the high power side i.e. the DC/DC converter side and the low power i.e. the FPGA electronic circuitry, greatly influenced the decision made when choosing an appropriate gate driver. The suitable gate driver for this design is chosen to be a 2ED020I12-F2 gate driver from Infenion. The gate driver is isolated galvanically and has a continuous isolation rating of 1.2 kV. However, the gate driver requires 5 V level gate signals although the FPGA generates 3.3 V level gate signals. Nonetheless, a TXS0108E voltage translator is used to level shift the gate signals from 3.3 V to 5 V required by the gate driver. The level shifter has no external components that should be designed and the voltage translation set-up is shown in Figure 4.22. The gate driver also provides several protection features like IGBT active shut down, desaturation protection and active Miller clamping . The isolation barrier in the gate driver circuitry implies that the high side and the low side be powered individually, thus two isolated 15 V power supplies are required by the driver. The complete set-up configuration from the FPGA device to the IGBT switches is shown in Figure 4.23. The high side, PWMH-1 and the low side PWML-1 are 3.3 V level signals generated by the FPGA and are translated to 5 V level by the TXS0108E level shifter. Moreover, the gate driver translates the 5 V signals to 15 V level gate signals namely high side PWMH-3 and the low side PWML-3. The 15 V level gate signals then drive the IGBT switches. The signals PWMH-3 and PWML-3 are complementary and have a dead time of 500 ns incorporated to ensure the the switches do not switch on at the same time as shown in Figure 4.24. The dead time is large enough to accommodate the propagation delays in the circuitry as well as the switching times of the IGBTs.

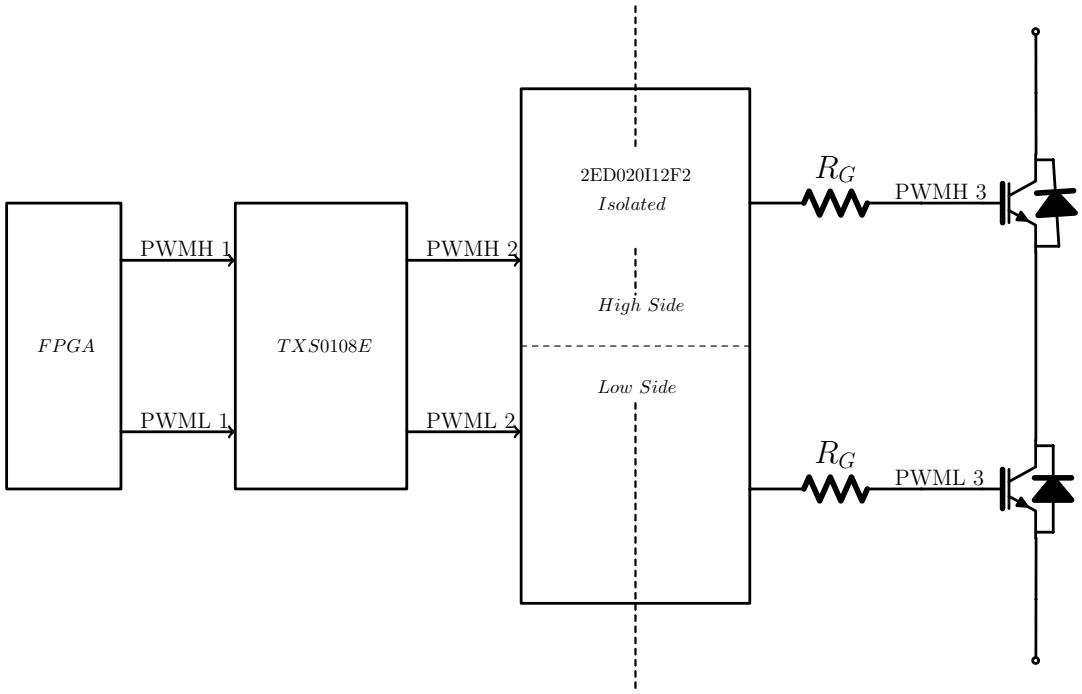

Figure 4.23: IGBT complete switching configuration

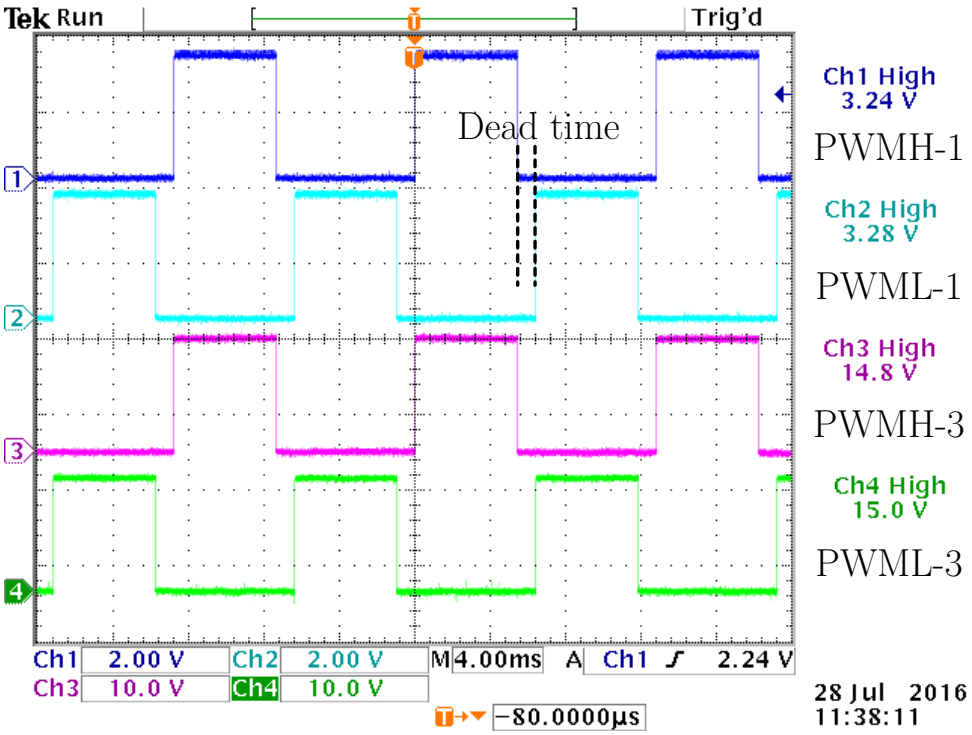

Figure 4.24: Gate driver PWM signals

4.6.1.1 Gate resistor

The IGBT switching times are changed by altering the gate resistors. The gate capacitance C_{GE}, is charged or discharged through the gate resistor R_G. Furthermore, this forms a first order RC circuit, thus the switching times are increased by increasing the R_G. The gate driver used can deliver a current of 1.5 A. The manufacturer of the gate driver recommends a gate resistance R_G of 10 Ω. An experiment is conducted in order to investigate the switching times and the voltage overshoot of the gating signals. Figure 4.25 shows the effect of the 10 Ω gate resistor on the gating signal. As can be observed from the figure, the turn on time of the switch S_1 is reasonable without any voltage overshoots. A few spikes and bumps are observed as the switch is turning on. This is also contributed by the gate signal resonating with the gate capacitance and the inductance of the driver's lead wires. For these reasons, the gate driver is placed very close to the IGBT in order to reduce the effect of stray inductance L_S. Therefore the behaviour in Figure 4.25, displayed by the S_1 gate signal when switching on, validates the 10 Ω gate resistor recommended by the manufacturer.

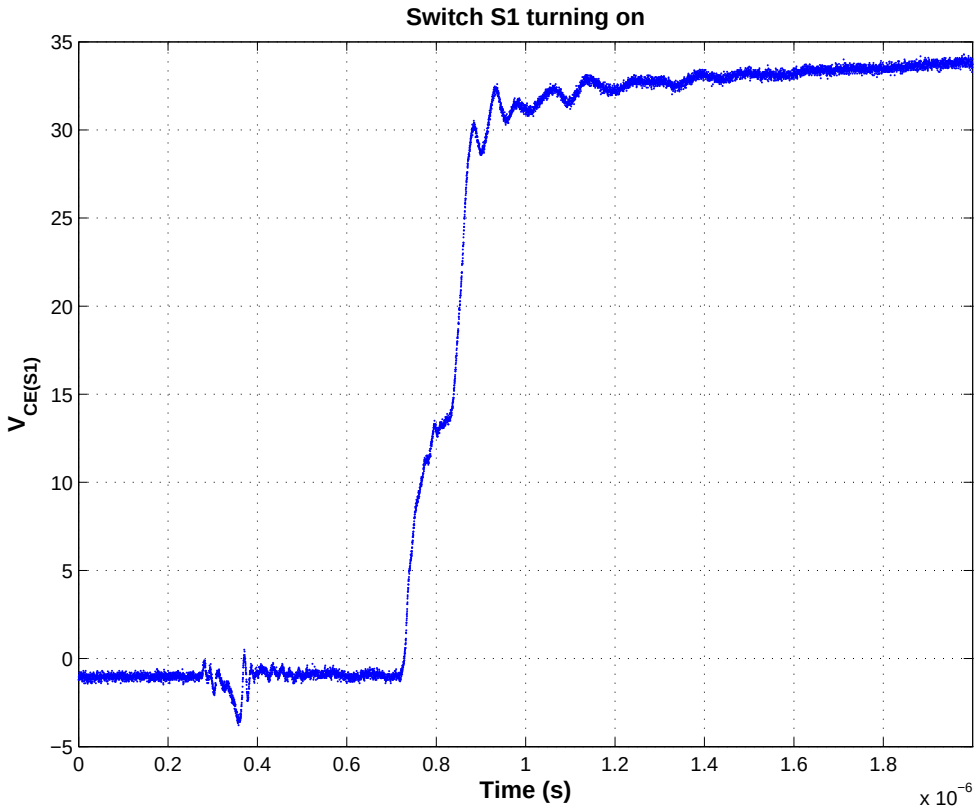

Figure 4.25: Gate resistance effect on IGBT turn on time

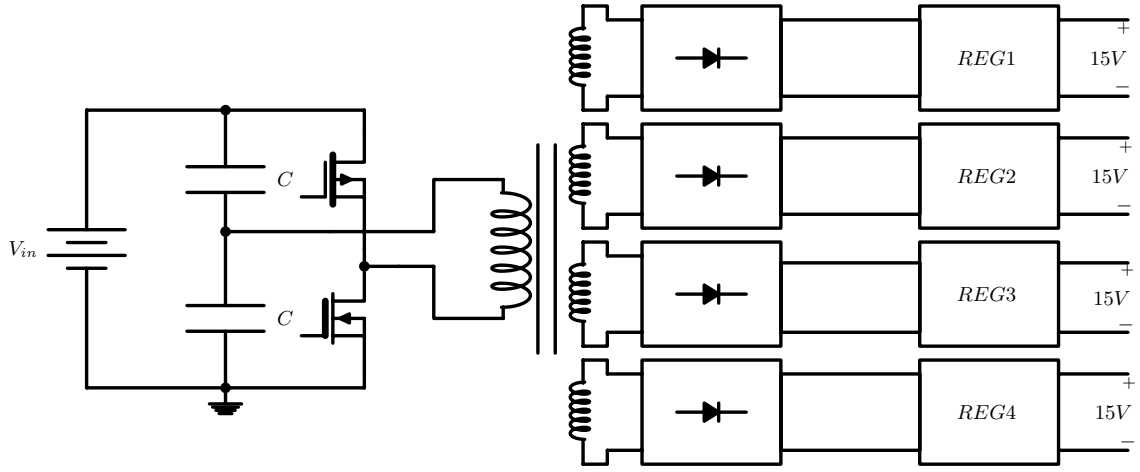

Figure 4.26: Isolated Power Supply Block diagram

4.6.2 Isolated Power Supply Design

The isolated power supply designed is responsible for powering the gate driver circuitry and the voltage sensor board. The Half bridge converter topology is employed in designing the isolated power supply. The block diagram of the isolated power supply is shown in Figure 4.26. The converter has a transformer with five windings, one primary winding and four secondary windings. Two of the secondary windings power outputs are used to power the gate driver circuitry and the remaining two are used to power the voltage sensor board. The half bridge converter does not saturate due to the balancing mechanism provided by the bus capacitors. Moreover, the polarity of the winding in the set-up configuration is also irrelevant, further simplifying the design and manufacturing process. The circuit is designed in such a way that the number of external components used is reduced, thereby reducing the cost and complexity of the PCB design shown in Figure 4.27.

The gate driver implemented in the design is the IR2184 chip from International Rectifier. The gate driver has a built-in bootstrap diode and the driver only requires three external components. The converter operates at a switching frequency of 20 kHz and a constant duty circle of 50%. The toroid used for the transformer is a $N27$ ferrite core material with an effective area of 51.26 mm^2 and the number of primary and secondary turns are 4 and 14, respectively. The input voltage of the converter at the primary side is 16 V and the output voltage at the secondary side is regulated to a constant 15 V by linear regulators.

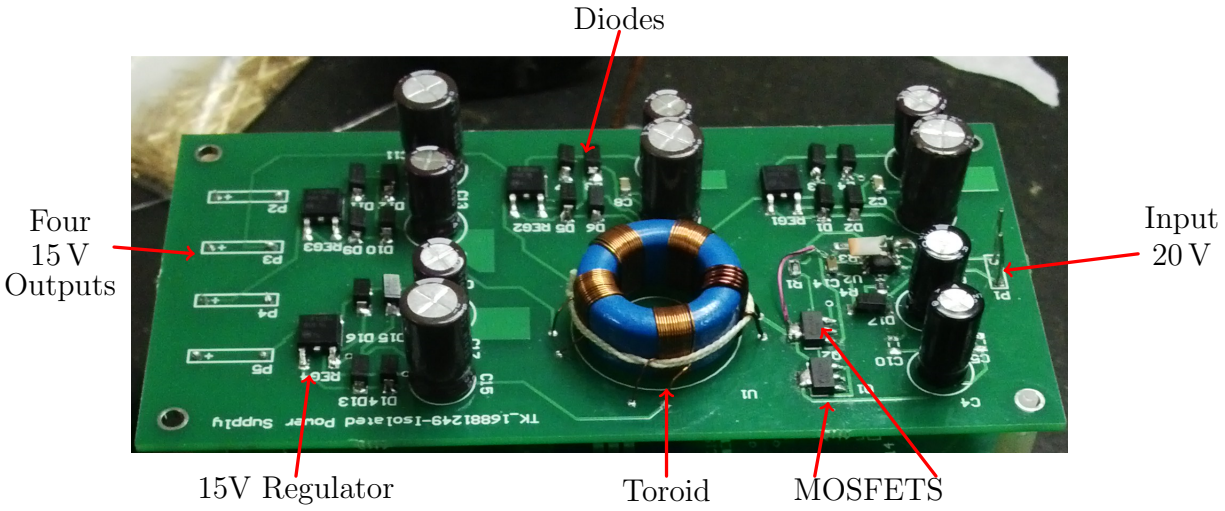

Figure 4.27: Isolated power supply board

4.7 Summary

In this chapter, the design and functionality of each sub-system is described. Several equations are derived that are used to design for the system's components e.g. bus capacitor, output filter capacitor and the inductor. Moreover the designs of the voltage and current sensors are described. Test results for the voltage sensor board show a 98.5% operational accuracy which is good enough for implementation in the SAE system. The characteristics of the amplifiers used for voltage sensing, do not affect the signal integrity during modulation, isolation and filtration. Therefore, the amplifiers offer excellent reliability and good high-frequency transient immunity.

Chapter 5

DC/DC converter controller design

The art of designing closed-loop controllers for power-electronic converters has been the topic of intense research since the dawn of Power Electronics. Many different models have been developed for designing closed loop controllers. In this chapter two design models that can be employed in order to design closed loop controllers are thoroughly investigated and then evaluated. The models evaluated are the small-signal model and the average model. Both models are implemented in designing a single closed loop current controller and a dual closed loop voltage and current controller. The dual closed loop structure implements an inner current control feedback-loop and an outer voltage control feedback-loop. The performance evaluation criteria for both the small-signal and the average models is based on each model's ability to accurately predict the stability margins of both of the closed loop controllers. The single and the dual closed loop controllers are designed so that they can be implemented individually by the Solar Array Emulator system. In the following sections, the average and the small-signal models are discussed and each model is used to design the single and the dual loop controllers.

5.1 Average model

The average linear model is a classical approach to designing closed loop controllers for pulse-width modulated converters. The average model is typically derived through the well-known method of Middlebrook and Ćuk [31]. Applying this state-space averaging technique to the pulse-width modulated converter results in an equivalent model in Figure 5.1, that is used for illustration. The pulse-width modulator and the switching stage of the converter are replaced by a gain equal to the input DC-bus voltage V_d of the converter as shown in Figure 5.1 where $G_c(s)$ is the compensator transfer function, $G_p(s)$ is the plant transfer function and $r(t)$ is the reference signal.

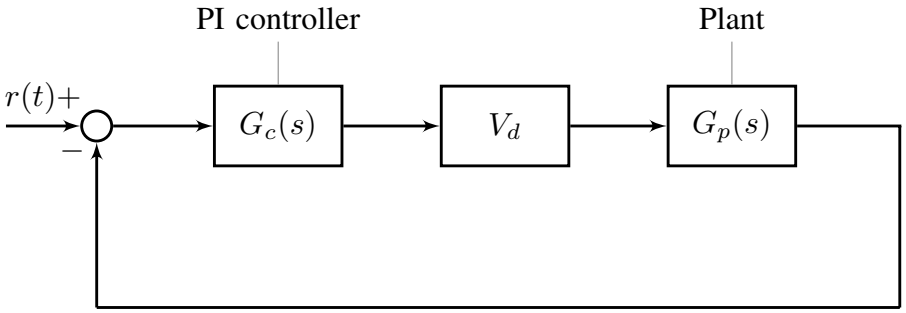

Figure 5.1: Equivalent model of a pulse-width modulated converter using the average model.

In this chapter, the average model is evaluated for accuracy in predicting the stability of closed loop controllers by means of root locus, Bode plots and time-domain simulations.

5.2 Small-signal model

In order to design a feedback controller with optimal performance, an accurate model of the pulse-width modulator is required. One way to analyse the stability of a feedback loop that contains non-linear components (in this case the pulse-width modulator) is to perform a perturbation analysis. Since a pulse-width modulated control loop is non-linear, it operates in a limit cycle. Figure 5.2 shows a typical analog feedback loop, in this case of a DC/DC converter that contains a single-edge naturally-sampled pulse-width modulator. This small-signal model is used in [32] to design a high-performance AC current regulator. In order to perform the perturbation analysis on the feedback loop, a small perturbation $r^*_{ss}(t)$ is superimposed on the reference signal $r^*_{ls}(t)$ as shown in Figure 5.2. This is done in order to analyse the input-output stability of the limit cycle. The question of stability of the underlying limit cycle comes down to whether the small perturbation causes the output signal of the control loop to grow or not. The output signal of the control loop is $r_{ls}(t) + r_{ss}(t)$, the input signal to the pulse-width modulator is $f_{ls}(t) + f_{ss}(t)$ and the output of the pulse-width modulator is $p_{ls}(t) + p_{ss}(t)$. By definition, the small-signal model is a linear model that describes the response of the non-linear component (the pulse-width modulator) to a small disturbance $f_{ss}(t)$ at its input.

Figure 5.3 shows the components of the input signal to the pulse-width modulator that consists of the large steady-state signal $f_{ls}(t)$ and the small perturbation signal $f_{ss}(t)$. The resulting PWM output signal $p_{ls}(t)+p_{ss}(t)$ is slightly shifted in time by a width of ΔT and this is due to the small perturbation signal $p_{ss}(t)$ as shown in Figure 5.3. The shift in time of the PWM output signal gives rise to a sequence of narrow rectangular pulses

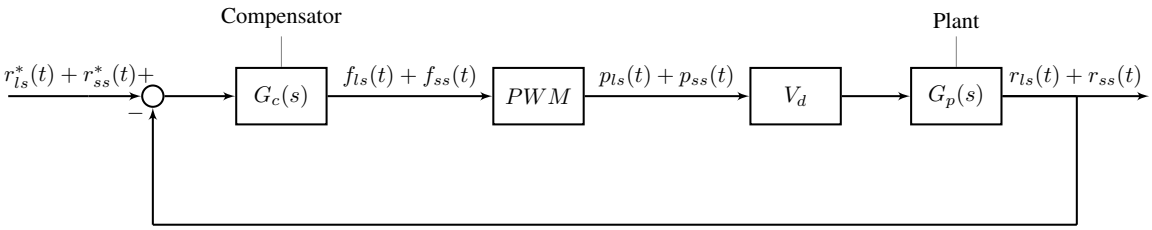

Figure 5.2: PWM feedback loop with perturbed reference $r^*_{ls}(t) + r^*_{ss}(t)$

with a height of one and a width of ΔT, represented by the narrow shaded rectangles in Figure 5.3. The distance between each narrow rectangular pulse is approximately equal to the switching period T_s. Therefore by definition, the small-signal model of the pulse width modulator can be said to be a mathematical model that produces a series of narrow rectangular pulses at the output of a pulse-width modulator if its input signal is the small perturbation signal $f_{ss}(t)$.

The narrow rectangular pulses are modelled in the form of an impulse train as shown in Figure 5.3. Each impulse has a strength equivalent to the area of the represented narrow rectangular pulse. Figure 5.4 depicts a zoomed view of one of the narrow rectangular pulses and the sampling point at time t_{sp} is the point where the large signal f_{ls} intersects the carrier signal. In order to determine the width of the pulse ΔT, the gradient $|\dot{r}_o|$ of $f(t)$, $f_{ls}(t) + f_{ss}(t)$, is taken at the sampling point t_{sp}. Note that the gradient of the carrier signal is equal to $\frac{1}{T_s}$ where T_s is equal to $\frac{1}{f_s}$. The width ΔT is illustrated in Equation 5.2.1.

$$\Delta T \approx \frac{f_{ss}(t_{sp})}{f_s - |\dot{r_o}|} \tag{5.2.1}$$

Since the height of the narrow rectangular pulse is equal to one, the area A of the rectangular pulse is shown in Equation 5.2.2.

$$A = \Delta T \approx \frac{f_{ss}(t_{sp})}{f_s - |\dot{r_o}|} \tag{5.2.2}$$

Equation 5.2.2 can be written in the form $A \approx f_{ss}(t_{sp}) K_{ss} T_s$. The small-signal gain of the pulse width modulator, denoted by K_{ss} is the equivalent gain of the impulse generator in the small-signal model of the pulse-width modulator. Equation 5.2.3 shows that the small-signal gain K_{ss} of a pulse-width modulator depends on the switching frequency f_s and the slope $|\dot{r}_o|$ of the input signal to pulse-width modulator prior to intersection with the carrier signal. It is shown in [33] that K_{ss} is accurate up to several times the f_s .

$$K_{ss} = \frac{f_s}{f_s - |\dot{r}_o|} \tag{5.2.3}$$

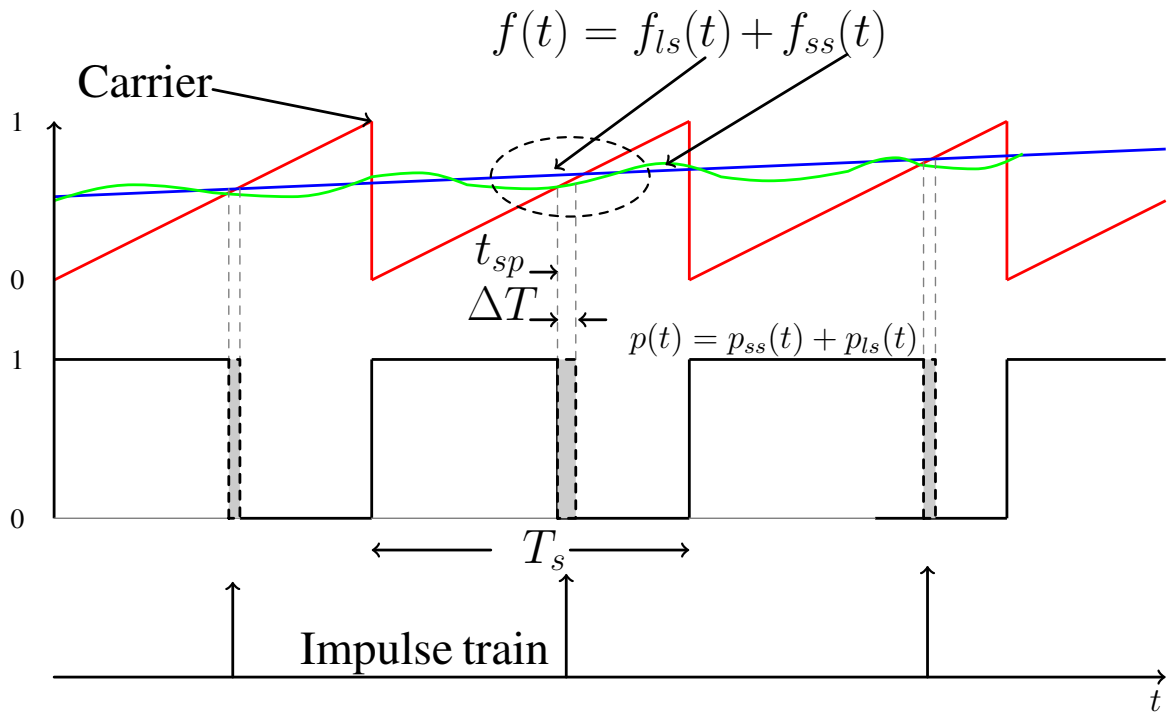

Figure 5.3: PWM small-signal model

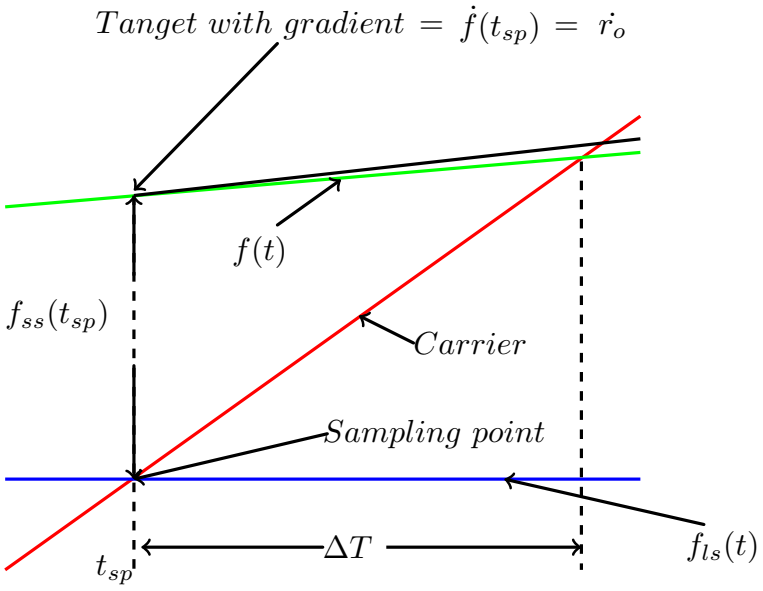

Figure 5.4: Zoomed view of the narrow rectangular pulse

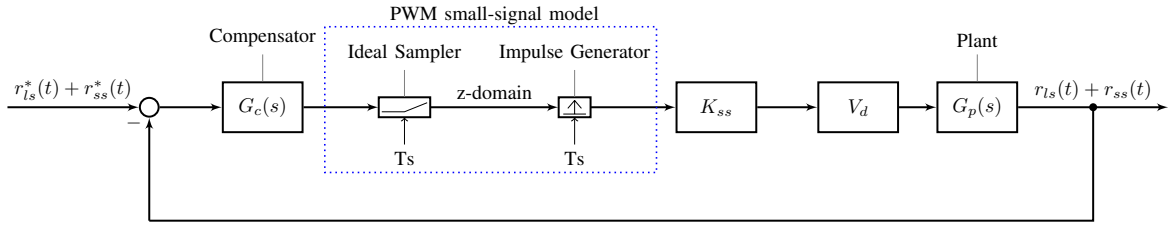

Figure 5.5: PWM small-signal model feedback loop with perturbed reference $r^*_{ls}(t)+r^*_{ss}(t)$

The pulse-width modulator PWM block in Figure 5.2 is replaced by the small-signal equivalent model, as shown in Figure 5.5. According to the small-signal model of the pulse-width modulator, a series of impulses are produced at every instance at which the input signal to the pulse-width modulator intersects the sawtooth carrier signal. The point of intersection is called the sampling point. According to [34], the small-signal model of the the pulse-width modulator is a sampling operation followed by an impulse generator with an equivalent small-signal gain K_{ss}. The sampling operation of the pulse-width modulator can be associated with discrete-time z domain. This discrete-time z domain is associated with the short link between the sampler and the impulse generator in small-signal model of the pulse-width modulator [32].

In order for the circuit to be characterised from the perspective of the z-domain, the link between the ideal sampler and the impulse generator is broken temporarily and the impulse generator emits a single impulse that characterises the surrounding linear circuit. At the same instant, the ideal sampler starts sampling with a sampling frequency equivalent to the switching frequency.

Let the open loop transfer of the feedback loop in Figure 5.5 be denoted by $G(s) = G_c(s)K_{ss}V_dG_p(s)$. The open loop transfer function is expanded into partial fractions in the form in Equation 5.2.4

$$G(s) = \sum_{n=1}^{N} \frac{A_n}{s + p_n} \tag{5.2.4}$$

where $-p_1$,$-p_2$, ..., p_N are s-domain poles assumed to lie in the left-half side of the complex plane. The discrete-time z-domain transfer function $G(z)$ is obtained by taking

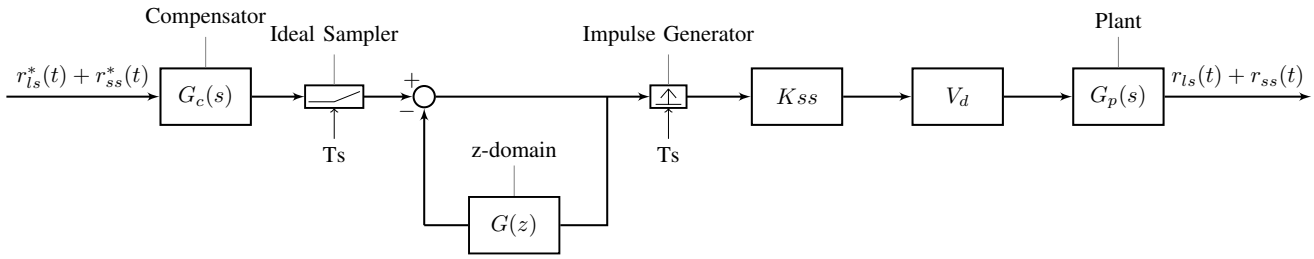

Figure 5.6: Equivalent block diagram of Figure 5.5

impulse response of $g(t)$ and is given by Equation 5.2.5.

$$\begin{aligned} G(z) &= T_s \sum_{k=1}^{\infty} g(kT_s - t_d) z^{-k} \\ &= T_s \sum_{n=1}^{N} A_n e^{p_n t_d} \left(\sum_{n=1}^{\infty} e^{-p_n T_s} z^{-k} \right) \\ &= T_s \sum_{n=1}^{N} A_n e^{p_n T_s} \frac{e^{-p_n T_s}}{z - e^{-p_n T_s}} \end{aligned} \tag{5.2.5}$$

The first sample of $g(t)(k = 0)$ is always zero as practical systems always have a small propagation delay hence, it is not included in the derivation of $G(z)$. The method of transforming the s-domain transfer function to the z-domain transfer function is known as the impulse invariant method [34]. The impulse invariant method maps the s-domain pole $-p_n$ into z-domain pole $e^{-p_n T_s}$. The s-domain poles are all assumed to be in the left half of the complex plane.

A block diagram manipulation is carried out on the closed loop controller, as shown in Figure 5.5 and the resulting feedback loop is shown in Figure 5.6. Figure 5.6 shows that the stability of the system is dependent on the stability of the z-domain feedback loop.

5.3 Mathematical modelling of the DC/DC converter

The DC/DC converter implemented by the SAE system is shown in Figure 5.7. The hardware design of the converter is discussed in greater detail in Chapter 4. The resistors r_L and r_c, in Figure 5.7, are inductor and capacitor parasitic resistances, respectively. In order to design and simulate a current or voltage regulator for the converter in Figure 5.7, a mathematical based description of the converter is firstly derived. In this section, the mathematical description of the converter is derived and the equations are then used in the later sections to design and model the single and dual closed loop controllers using

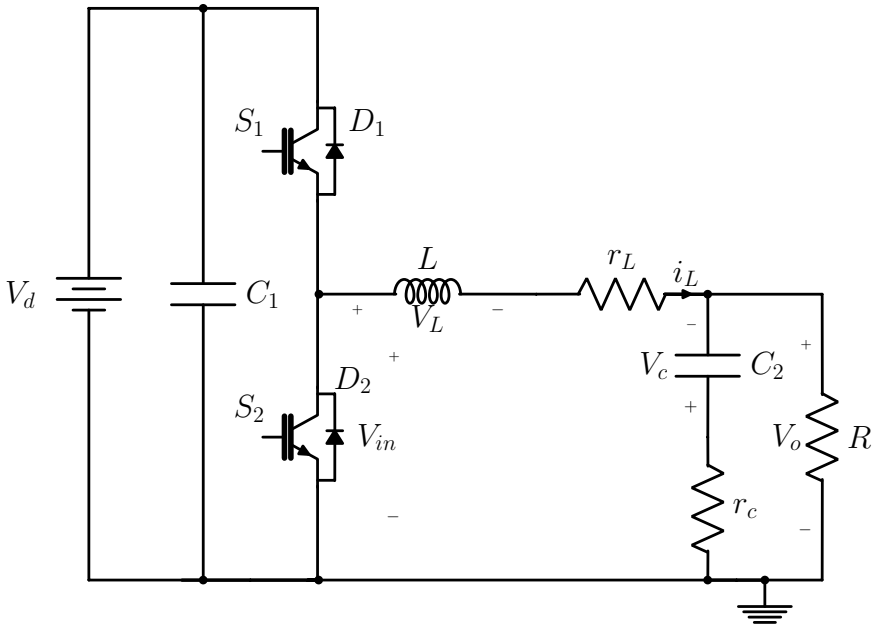

Figure 5.7: Bi-directional synchronous buck converter

both the average and the small-signal models.

By analysing the circuit in Figure 5.7 the following equations are obtained:

$$v_{in}(t) = L\frac{di}{dt} + r_L i_L(t) + v_c(t) + r_c C_2 \frac{dv_c}{dt} \tag{5.3.1}$$

Taking the Laplace transform of Equation 5.3.1 gives the following equations.

$$\begin{aligned} V_{in}(s) &= sLI_L(s) + r_L I_L(s) + V_c(s) + sr_c C_2 V_c(s) \\ &= I_L(s)(sL + r_L) + V_c(s)(sr_c C_2 + 1) \end{aligned} \tag{5.3.2}$$

$$I_L(s) = \frac{V_{in}(s) - V_c(s)(sr_c C_2 + 1)}{sL + r_L} \tag{5.3.3}$$

Moreover:

$$V_c(s) + sr_c C_2 V_c(s) = RI_L(s) - sRC_2 V_c(s)$$

$$V_c(s) + sr_c C_2 V_c(s) + sRC_2 V_c(s) = RI_L(s)$$

Therefore,

$$V_c(s) = \frac{RI_L(s)}{sC_2(R + r_c) + 1} \tag{5.3.4}$$

The output voltage is given by:

$$V_o = R(I_L(s) - sC_2 V_c)$$

Substituting for V_c, yields:

$$V_o(s) = \frac{R(sC_2 r_c + 1)I_L(s)}{sC_2(R + r_c) + 1} \tag{5.3.5}$$

5.4 Single loop current controller

The single loop current controller that regulates inductor current for the converter in Figure 5.7 is designed. The average and the small-signal model are discussed in greater detail in Section 5.1 and Section 5.2, respectively. Each model is analysed and evaluated for accuracy in designing and predicting the stability margins of the single loop current controller.

5.4.1 Single loop controller design using the average model

The single closed loop control system in Figure 5.8 is based on the mathematical description of the converter shown in Figure 5.7 and derived in Section 5.3. The single closed loop current controller regulates the inductor current. The average model and the open loop transfer function of the closed loop systems is shown in Equation 5.4.1

$$G(s) = \frac{G_c(s)G_1(s)V_d}{1 + G_1(s)G_2(s)} \tag{5.4.1}$$

where the transfer functions namely $G_1(s)$ and $G_2(s)$ shown in Equation 5.4.2 and Equation 5.4.3, respectively. $G_1(s)$ and $G_2(s)$ are obtained through mathematical modelling of the synchronous buck converter discussed in the previous section.

$$G_1(s) = \frac{1}{sL + r_L} \tag{5.4.2}$$

$$G_2(s) = \frac{R(sC_2r_c + 1)}{sC_2(R + r_c) + 1} \tag{5.4.3}$$

The transfer function $G_c(s)$ is the Proportional-integral (PI) controller for optimal control of the feedback loop. Small values of K_p and K_i, valued at 0.0048 and 0.35 Hz, respectively, are used for the PI controller. These values are the same as the values of K_p and K_i designed using the small-signal model in Section 5.4.2.1. The reason for using the same parameters when implementing both the average and the small-signal model is to ensure a fair evaluation between between both models. The open loop transfer function $G(s)$ in Equation 5.4.1, is used to plot the root locus and the Bode plot of the closed loop controller in order to analyse the stability margins.

5.4.1.1 Average model verification and simulation results

An analysis is conducted on the root locus in Figure 5.9 and the Bode plot in Figure 5.10 to determine the stability margins of the system. It is observed from the root locus and the Bode plot that the closed loop poles are located in the left half of the complex plane and the system has an infinite gain margin. However, such an observation does not

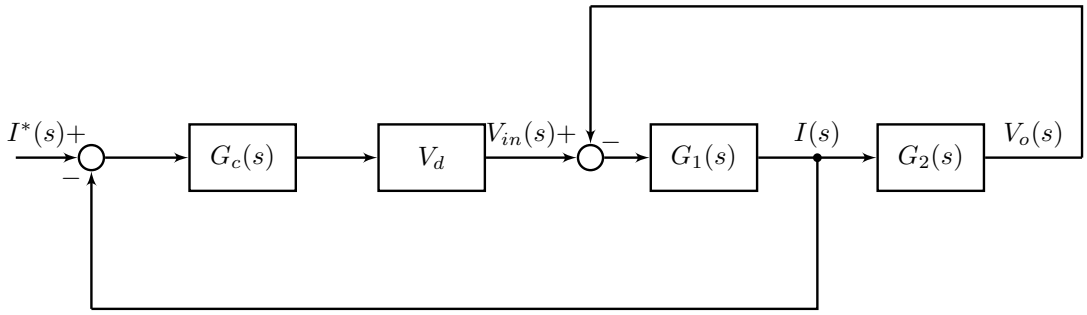

Figure 5.8: Single loop current controller using the average model

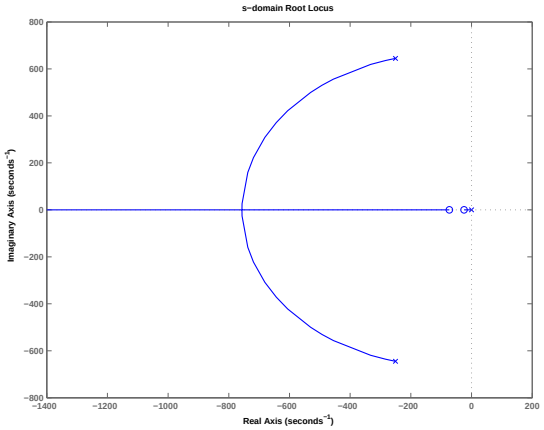

Figure 5.9: Root locus of the single loop controller designed using the average model

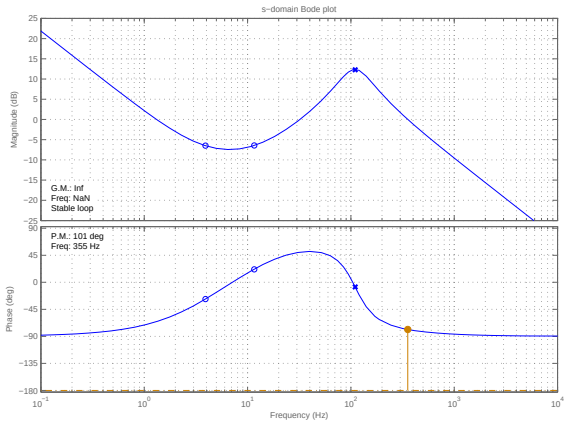

Figure 5.10: Open-loop Bode plot of the single loop controller designed using average model

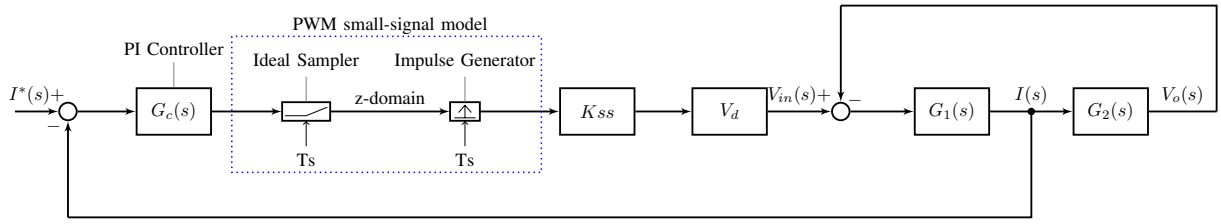

Figure 5.11: z-domain model of PWM current regulator

accurately predict the stability margins of the single closed loop controller as practical systems do not have an infinite gain margin, as will be shown later.

5.4.2 Single loop controller design using the small-signal model

In this section the small-signal model previously discussed is used to design the single closed loop current controller. Figure 5.11 shows the z-domain model of the single loop

current controller for the synchronous buck converter. The transfer functions namely $G_1(s)$ and $G_2(s)$ are shown in Equation 5.4.2 and Equation 5.4.3, respectively. The open loop transfer function of the z-domain single loop controller in Figure 5.11 is given by Equation 5.4.4. The block diagram in Figure 5.11 is manipulated to obtain a block diagram equivalent to Figure 5.2. $G_c(s)$ is a PI controller that has values of K_p and K_i that need to be designed for.

$$G(s) = \frac{G_c(s)G_1(s)V_dK_{ss}}{1 + G_1(s)G_2(s)} \tag{5.4.4}$$

5.4.2.1 PI controller design for the single closed loop controller

An algorithm is developed to design the K_p and K_i values for the PI controller $G_c(s)$. The algorithm developed is based on the flow diagram shown in Figure 5.12. A nested for loop is designed with an outer loop incrementing the values of K_p and the inner loop incrementing the values of K_i, as shown in Figure 5.12. The nested for loop iterates sequentially and during each iteration, the continuous time-domain open loop transfer function $G(s)$ is transformed to the discrete-time domain transfer function $G(z)$ using the impulse invariant method derived in Section 5.2. Remember that the small-signal model employs z-domain techniques to design controllers. The transfer function $G(z)$ is used to determine the location of the z-domain closed loop poles. Therefore for each iteration, the corresponding values of K_p and K_i that result in the z-domain closed loop poles being located within the unit circle are stored. Moreover, the values of K_p and K_i that results in the z-domain closed loop poles being located outside of the unit circle are also stored. Therefore, two regions exist that define the range of values of K_p and K_i and that result in z-domain poles being located within or outside the unit circle. Those that are within the unit circle ensure the stability of the controller and those that are outside the unit circle will make the controller unstable. The stable and unstable regions are shown in Figure 5.13.

5.4.2.2 Small-signal model verification and simulation results

The values of K_p and K_i for the PI controller are chosen as 0.0048 and 0.35 Hz from the plot in Figure 5.13. These values are chosen from the whole range because by using these values, the output current from the closed loop controller is critical damped i.e no overshoots that causes problem in practical implementation. The z-domain open loop transfer function $G(z)$ is used to determine the root locus and the Bode plot shown in Figure 5.14 and Figure 5.15, respectively. The closed loop poles of the z-domain root locus are all located within the unit circle. It can be observed that one pole is dominant as the other two poles are each placed close to zeros, hence the two poles have very small

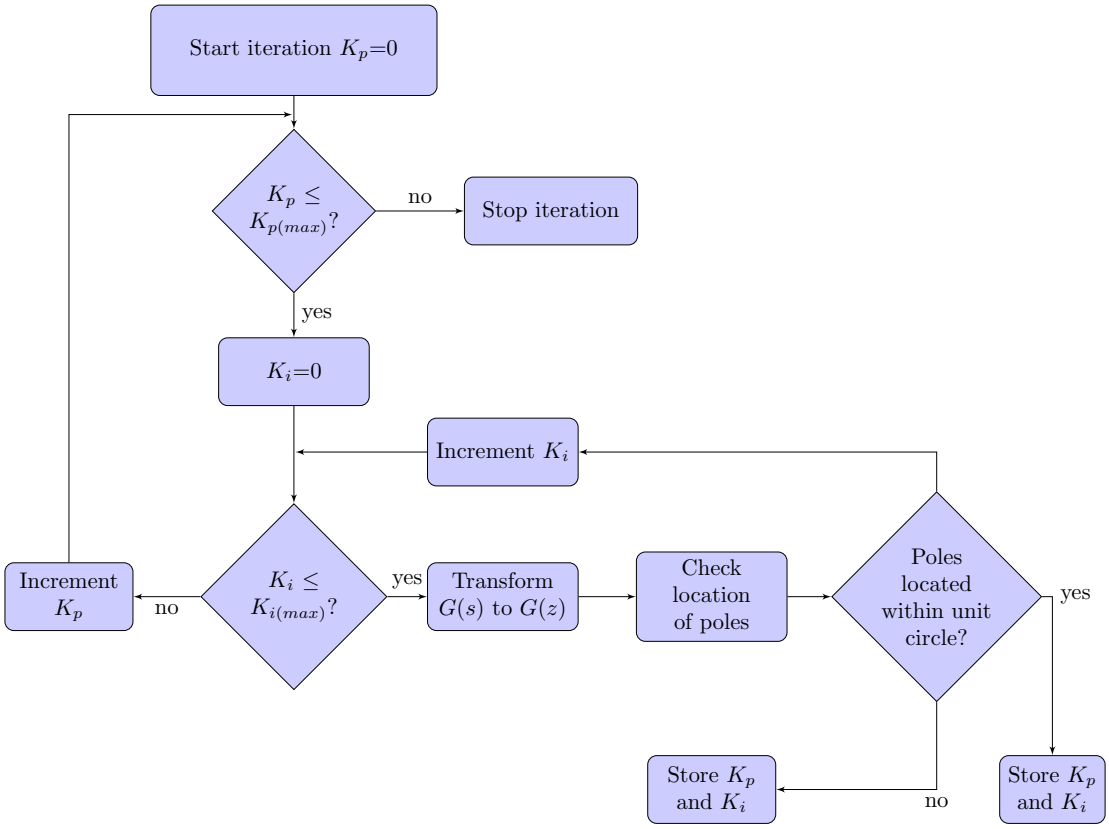

Figure 5.12: PI controller design flow diagram

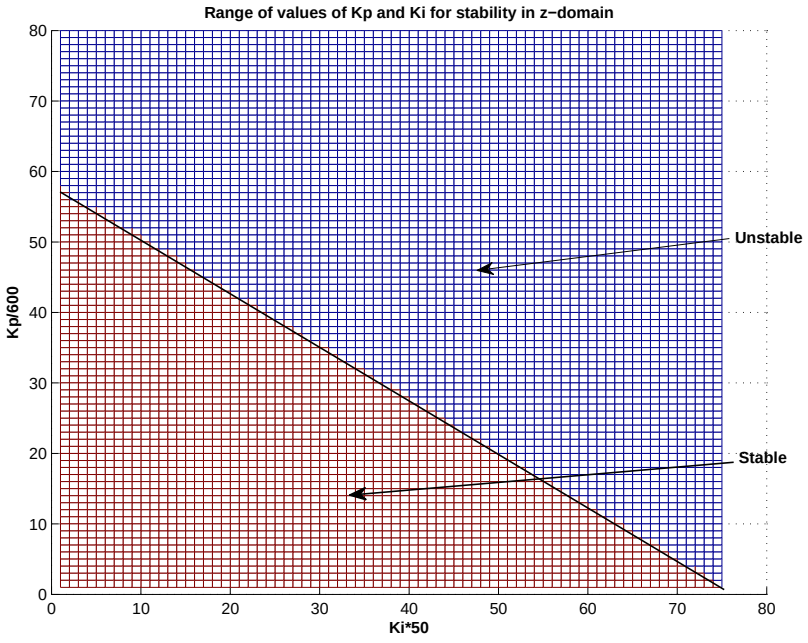

Figure 5.13: Range of values of K_p and K_i for stability

influence on the time domain behaviour of the system. The gain and phase margins are 25.8 dB and 98.5° respectively.

Simulations of the closed control system in Figure 5.11 were carried out in Matlab® in order to verify the validity and accuracy of the small-signal modelling approach in predicting the stability margins.

In order to analyse the stability of the single closed loop controller designed by means of the small-signal model, an algorithm is developed that simulates the buck converter with the PI controller, shown in Figure A.1. A similar approach is used in [35]. The algorithm developed is based on the state space representation of the synchronous buck converter with the PI controller. The state space representation is derived in Appendix A.1. According to the developed algorithm, an additional loop gain K_a is inserted into the closed loop and gradually increased. The behaviour of the duty cycle in Figure 5.16 is observed over time as the additional loop gain is gradually increased. The simulated bifurcation diagram shown in Figure 5.16, is based on the developed algorithm.

Bifurcation diagrams are regarded as useful tools in power electronics to analyse stability of closed loop systems [35]. The point labelled as the bifurcation point indicates the point where the single closed loop controller goes unstable. The behaviour of the small-signal gain K_{ss} is dependent on the gradient of the compensator output signal prior to intersection with the carrier signal, as previously discussed in Section 5.2. Therefore, as the additional loop gain is ramped up, the ripple gradient also increases, which in turn reduces the small-signal gain K_{ss}. The actual loop gain of the closed loop controller is therefore the product of the additional loop gain K_a and the small-signal gain K_{ss}. Figure 5.17 shows the actual loop gain as a function of the additional loop gain K_a. In Figure 5.17, the occurrence of the bifurcation point is noticed just after the actual loop gain plot crosses the theoretical gain margin plot. The value of the actual loop gain where the first bifurcation point is noticed is 19.51. This value closely approximates the theoretical gain margin of 19.4984 predicted in the Bode plot in Figure 5.15. This therefore indicates that the small-signal z-domain model predicts the stability margins of the single loop current controller with a greater degree of accuracy.

To further verify the validity of the small-signal model, a reference current of 18 A is given at the input of the single loop controller. Figure 5.18 shows that the single loop current controller is able to regulate the inductor current to an average of 18 A. Using a resistive load of 40 Ω, the output voltage is simulated as 720 V, as shown in Figure 5.19.

Moreover, the designed closed loop controller is simulated to track the response to a reference step. The reference is stepped from 2 A to 4 A and the simulated tracking response is shown in Figure 5.20. At the occurrence of the step, the current controller enters PWM saturation and then quickly settles with no error once the PWM switching

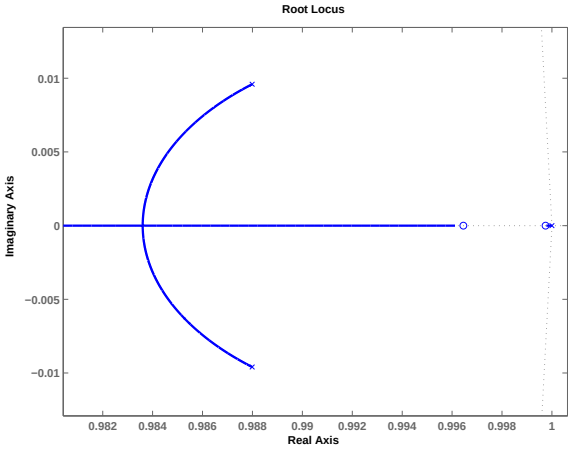

Figure 5.14: Root Locus of the single loop current controller

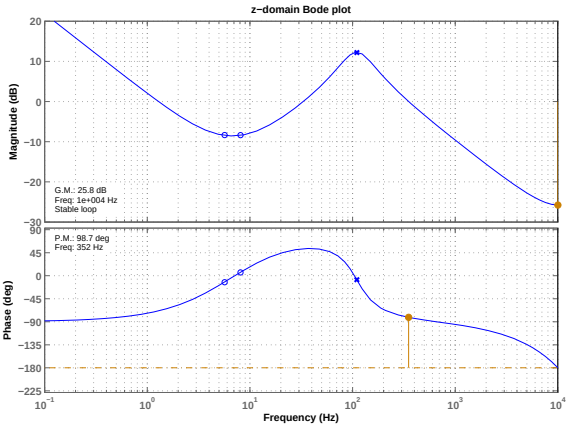

Figure 5.15: z-domain open loop Bode plot of the single loop current controller

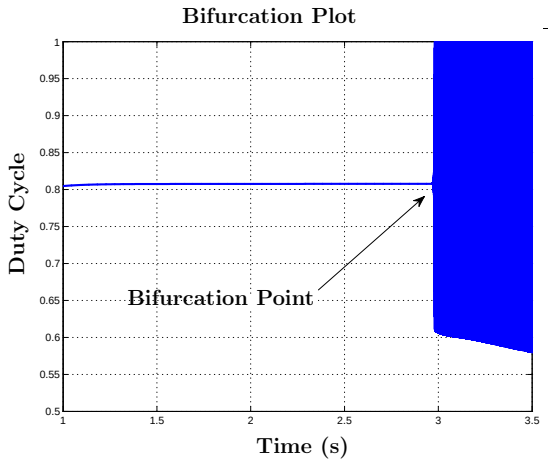

Figure 5.16: Simulated bifurcation diagram of the single loop current controller

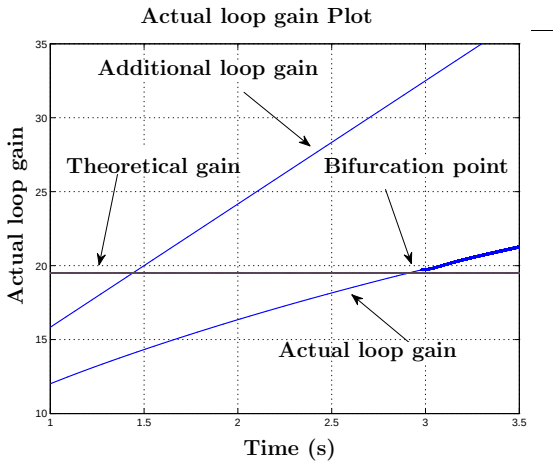

Figure 5.17: Actual loop gain plot of the single loop current controller

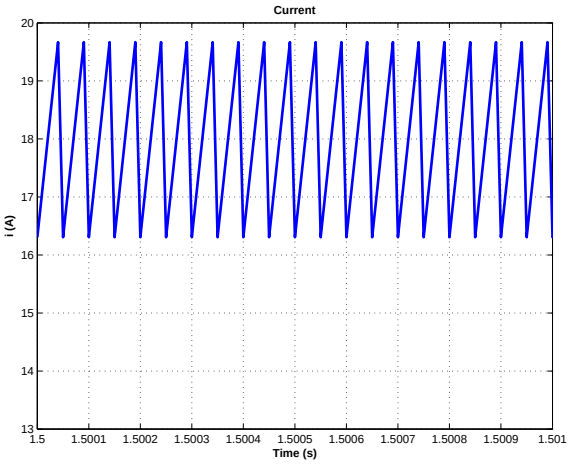

Figure 5.18: Simulated inductor Current of the single loop current controller

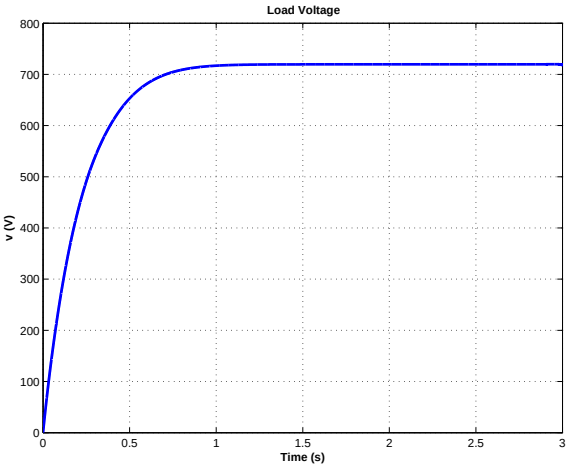

Figure 5.19: Simulated load Voltage of the single loop current controller

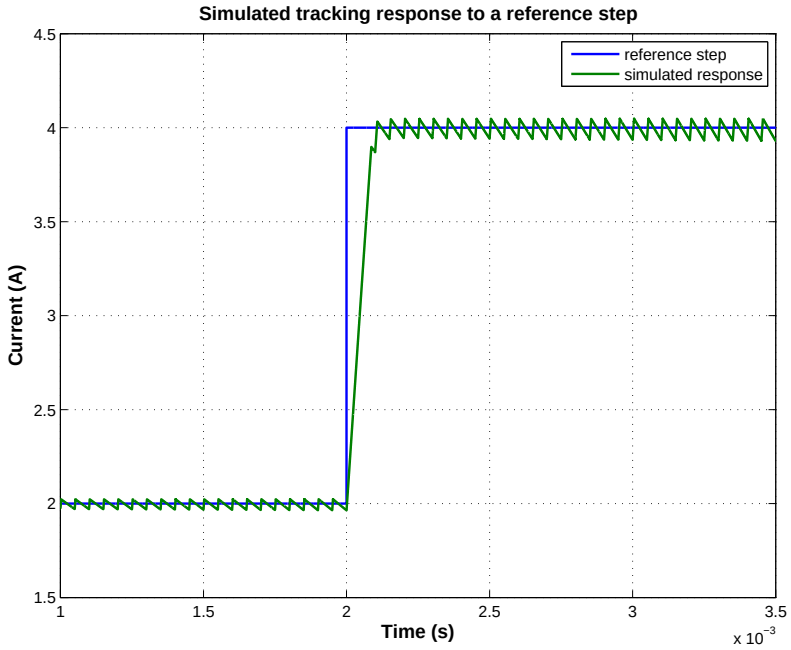

Figure 5.20: Simulated tracking response to reference step

recommences. This validates the small-signal model approach adopted.

5.4.2.3 Practical experiment of the single loop current controller

An experimental system with parameters in Table 5.1 was set up in order to test the control algorithm developed for the single loop controller designed through the use of the z-domain methods. The control algorithm was implemented on the FPGA device in order to regulate the inductor current of the DC/DC converter designed in Chapter 4.

Table 5.1: System parameters

DC-bus voltage (V_d)	20 V
Filter Inductance (L)	2.08 mH
Load Resistance (R)	5 Ω
Inductor ESR (r_l)	0.4 Ω
Switch frequency (f_s)	20 kHz
Sampling frequency (f_{sample})	50 MHz
Filter capacitance (C)	5000 µF
Capacitor ESR (r_c)	0.6 Ω

Figure 5.21 shows the experimental result of the measured inductor current when the reference current is 2.5 A. In addition, Figure 5.21 shows the measured inductor current when the system is responding to a step in reference current from 1.5 A to 2.5 A. The

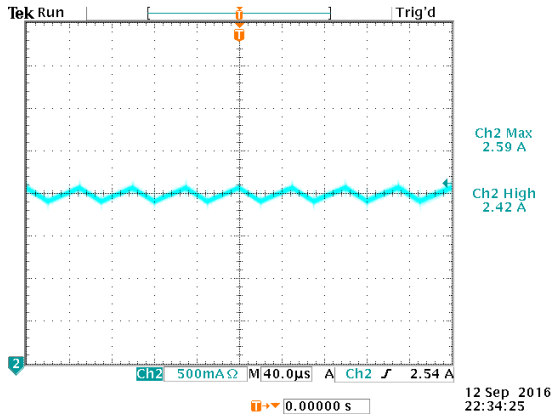

Figure 5.21: Measured response to a constant input

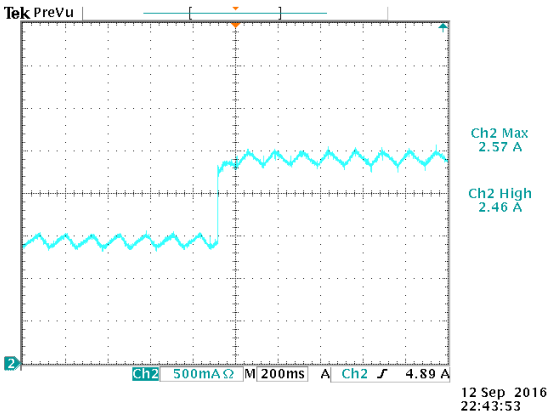

Figure 5.22: Measured response to a step input

practical measurements strongly agree with the simulated results thereby validating the use of the z-domain methods in designing the single loop current controller.

5.5 Dual loop voltage and current controller

The classical approach to control the output voltage of a buck converter is to use an inner current control loop and an outer voltage control loop [36]. This dual loop structure offers a number of advantages and simplifies the design of the controller. Two models discussed previously, namely the average model and the small-signal model, are employed in designing the dual loop voltage and current controller.

5.5.1 Designing the dual loop controller using the average model

The dual-loop continuous-time controller in Figure 5.23 consists of an inner-loop current controller and an outer-loop voltage controller. A block diagram manipulation is carried out on Figure 5.23 in order to determine the open loop transfer function of the system. Both the inner current and outer voltage control loops are based on PI controllers. The transfer functions $G_1(s)$ and $G_2(s)$ are obtained from the mathematical model of the converter derived in Section 5.3 and are given in Equation 5.4.2 and Equation 5.4.3, respectively. The open-loop transfer function of the model in Figure 5.23, is described by Equation 5.5.1.

$$G(s) = \frac{G_{c1}(s)G_{c2}(s)G_1(s)G_2(s)V_d}{G_1(s)G_2(s) + G_1(s)G_{c2}(s)V_d + G_{c2}(s)G_1(s)G_2(s)V_d + 1} \tag{5.5.1}$$

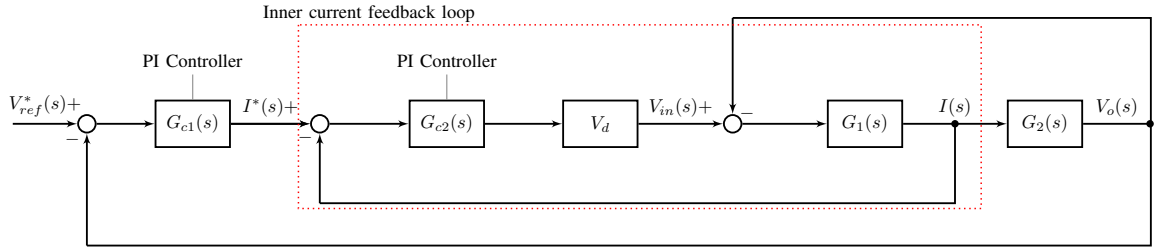

Figure 5.23: Continuous-time dual voltage and current loop controller

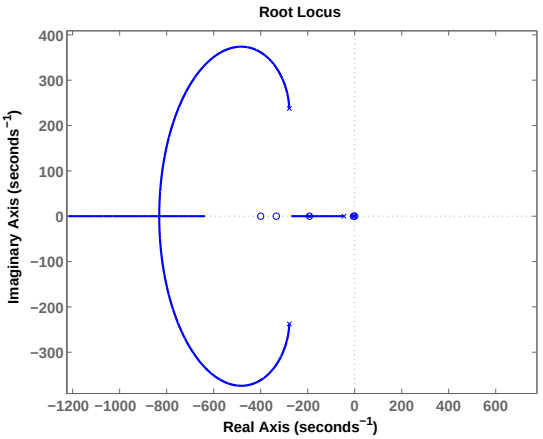

Figure 5.24: Continuous-time domain root locus for the dual loop controller

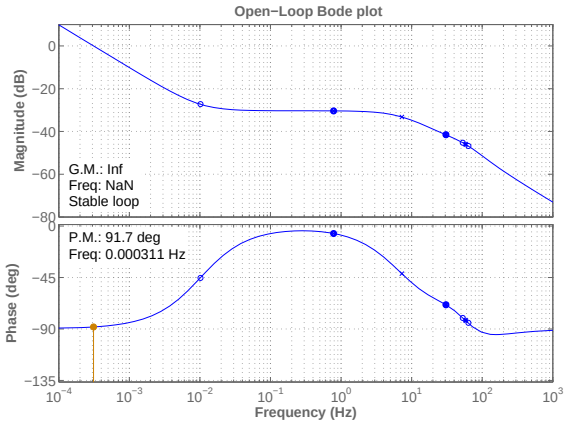

Figure 5.25: Corresponding continuous-time domain open loop Bode plot

5.5.1.1 Average model verification and simulation results for the dual loop controller

The PI controllers in Figure 5.23 namely $G_{c1}(s)$ and $G_{c2}(s)$ have the same values of K_p and K_i as those designed using the small-signal model. The design strategy for these values is described later in Section 5.5.2.1. The reason for using the same parameters when implementing both the average and the small-signal model is to ensure a fair evaluation between both models. The values of K_p and K_i for the PI controller $G_{c1}(s)$ are 0.0312 and 0.002 Hz, respectively. Moreover, for the PI controller $G_{c2}(s)$, the values of K_p and K_i are 0.000 175 and 0.07 Hz, respectively. In order to predict the stability margins of the system using the average model, the root locus and the Bode plot in Figure 5.24 and Figure 5.25 are analysed. According to the root-locus plot, all the closed-loop poles are located in the left half of the complex plane irrespective of the value of the loop gain, implying an infinite gain margin. However, it is shown later that the controller does in fact have a finite gain margin.

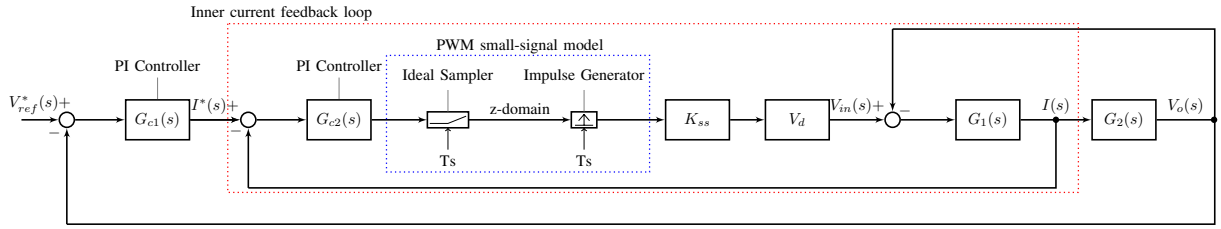

Figure 5.26: z-domain model of PWM dual loop voltage controller

5.5.2 Dual loop controller design using the small-signal model

Figure 5.26 shows the small-signal z-domain model of PWM embedded on the dual loop controller. The open loop transfer function of the dual loop controller is given by Equation 5.5.2.

$$G(s) = \frac{G_{c2}(s)V_d K_{ss} G_1(s)}{1 + G_1(s)G_2(s)} \left(1 + G_{c1}(s)G_2(s)\right) \tag{5.5.2}$$

Transfer functions, namely $G_1(s)$ and $G_2(s)$ are given in Equation 5.4.2 and Equation 5.4.3, respectively. A strategy is implemented in order to design the two PI controllers in Figure 5.26, namely $G_{c1}(s)$ and $G_{c2}(s)$ that both have K_p and K_i values.

5.5.2.1 PI controller design for the dual closed loop controller

A flow diagram in Figure 5.27 is used to develop an algorithm that designs the K_p and K_i values for both PI controllers. According to the flow diagram, K_{p1} and K_{i1} belong to PI controller $G_{c1}(s)$ and K_{p2} and K_{i2} belong to $G_{c2}(s)$. A nested for loop is created with an outer loop that incrementing small values of K_{p1} and three inner nested loops that increments small values of K_{i1}, K_{p2} and K_{i2}, respectively. The nested loops iterate sequentially and during each iteration, the time-domain open loop transfer function $G(s)$ in Equation 5.5.2 is transformed to discrete domain transfer function $G(z)$. The resulting closed loop transfer function in z-domain is checked whether its closed loop poles are located in the unit circle of the z-domain root locus, indicating stability in the z-domain. Remember that the small-signal model employs z-domain techniques hence the stability of the controller is determined by the stability of the z-domain feedback loop. The iteration process is repeated until the corresponding values of K_{p1}, K_{i1}, K_{p2} and K_{i2} result in the z-domain closed loop poles being located in the unit circle of the root locus. Once these values are obtained, the iteration process is stopped.

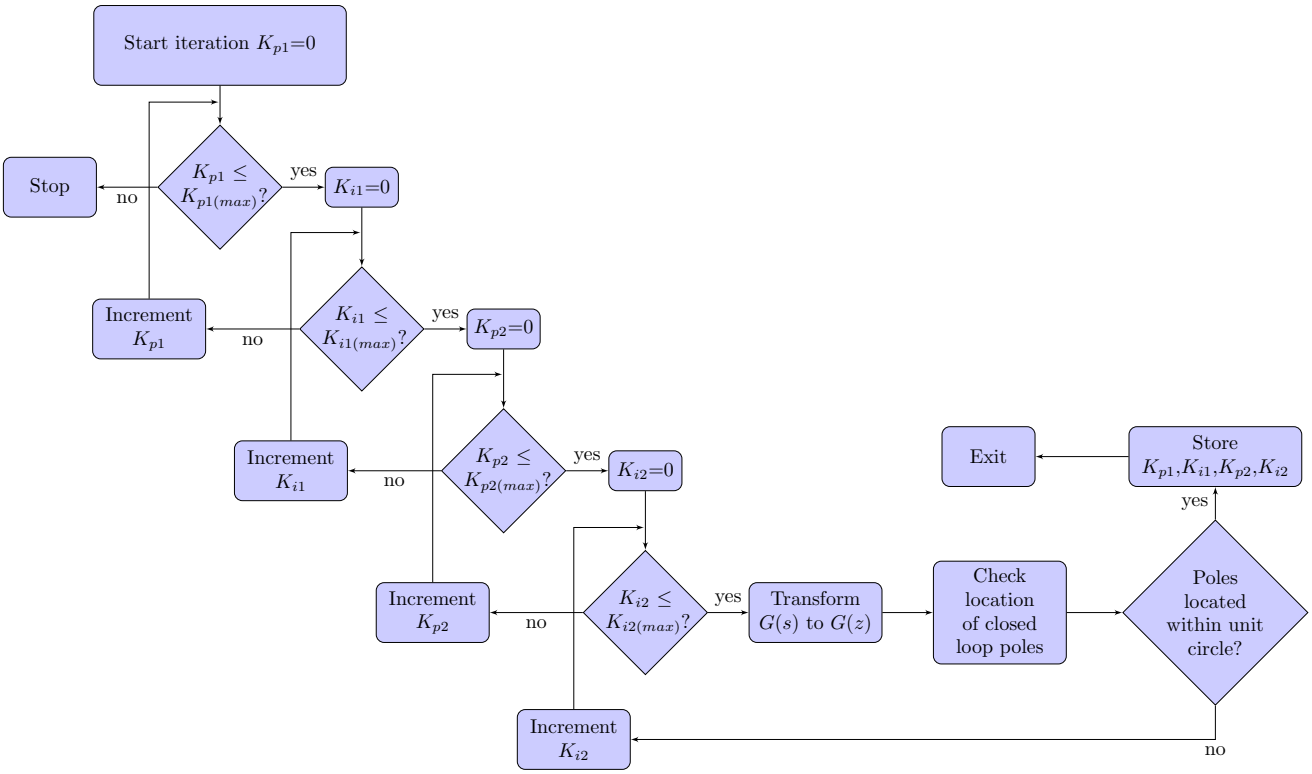

Figure 5.27: PI controllers design flow diagram for the dual closed loop controller

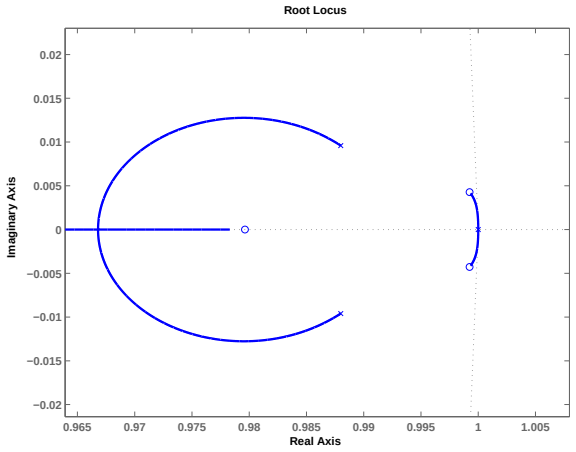

Figure 5.28: z-domain root Locus for the dual loop controller

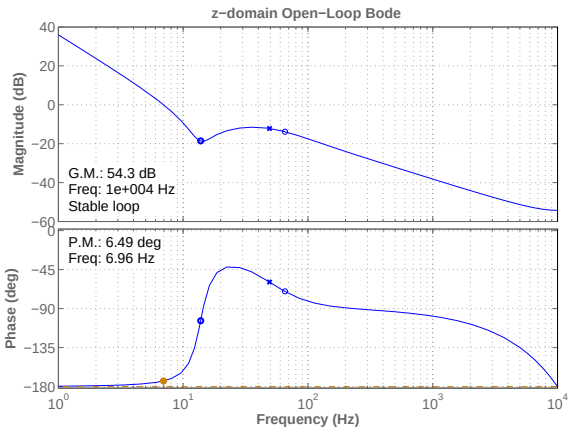

Figure 5.29: Open loop Bode plot for the dual loop controller

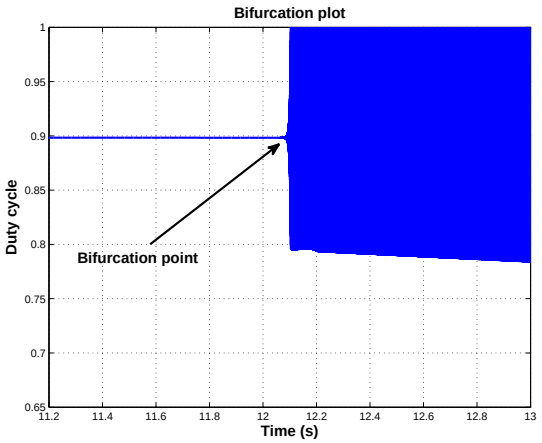

Figure 5.30: Bifurcation diagram of the dual loop controller

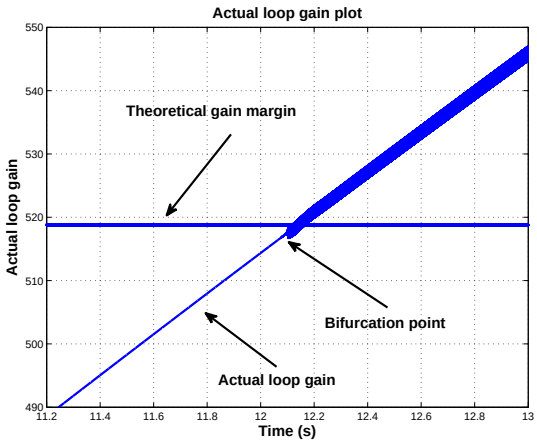

Figure 5.31: Actual loop gain plot of the dual loop controller

5.5.2.2 Small-signal model verification and simulation results

After the iteration process described above is stopped, the values of K_p and K_i for PI controller $G_{c1}(s)$, are determined as 0.0312 and 0.002 Hz, respectively and for the PI controller $G_{c2}(s)$, the values are 0.000 175 and 0.07 Hz, respectively. Figure 5.28 shows the root locus with poles located within the unit circle and Figure 5.29 shows a Bode plot with a theoretical gain margin of 54.3 dB for the dual loop controller.

Simulations were conducted in Matlab® in order to verify the validity and accuracy of the z-domain small-signal model in predicting the stability margins of the dual loop controller. An algorithm to simulate the dual closed loop controller is developed based on the state space representation of the dual closed loop controller derived in Appendix A.2. Based on the developed algorithm, an additional gain K_a is inserted into the inner current feedback loop in Figure 5.26. The value of K_a is ramped up slowly and the behaviour of the duty cycle is analysed. Figure 5.30 shows the growth of the duty cycle over time. A bifurcation point indicating the point where the dual loop controller becomes unstable is observed at 12.1 s. Figure 5.31 indicates a gradual increase in actual loop gain with an increase in additional loop gain. As previously discussed, the actual loop gain is the product of additional loop gain K_a and small-signal gain K_{ss}. From the point labelled bifurcation point and onwards in Figure 5.31, the behaviour of the actual loop gain changes and becomes random, indicating the point where the dual loop controller becomes unstable. A bifurcation point in Figure 5.31 is observed just before the actual loop gain crosses the theoretical gain margin predicted by the Bode plot in Figure 5.29.

Therefore the gain margin predicted by the small-signal model closely approximates the theoretical gain margin. Remember that the average model predicted an infinite gain margin.

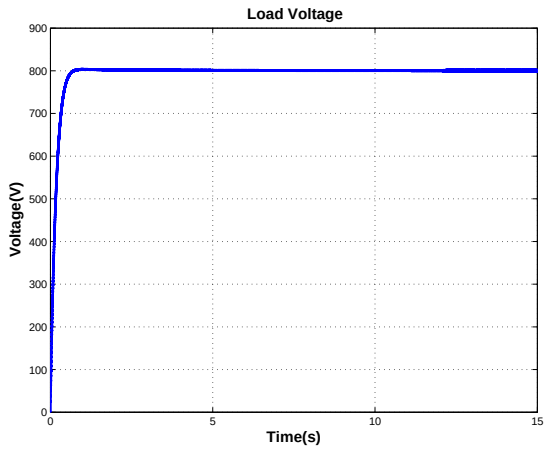

Figure 5.32: Simulated voltage tracking using the dual loop controller

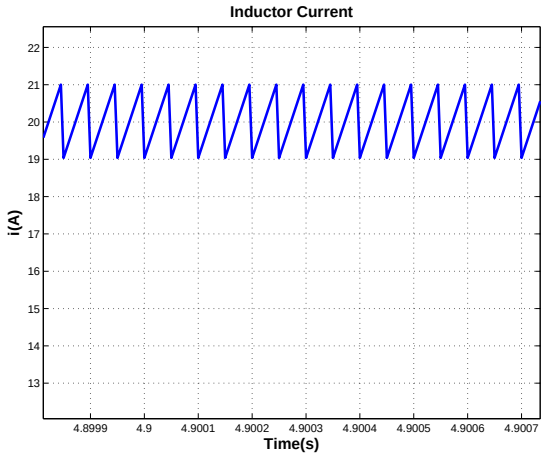

Figure 5.33: Simulated inductor current using the dual loop controller

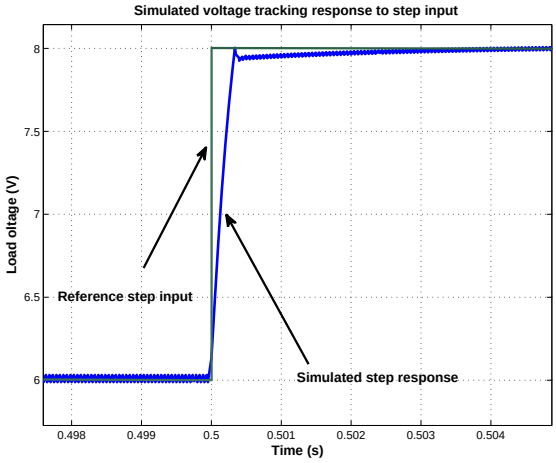

Figure 5.34: Simulated step input voltage tracking of the dual loop controller

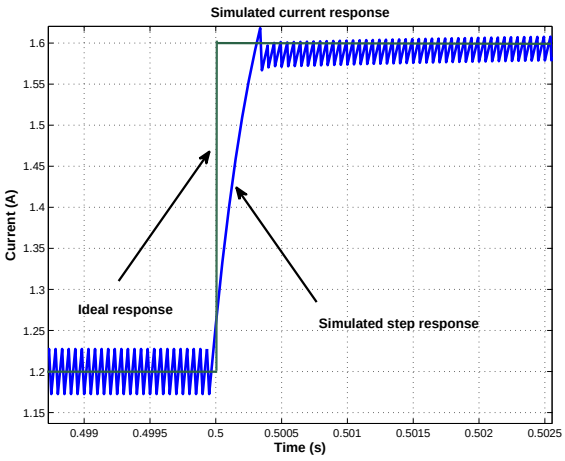

Figure 5.35: Simulated inductor current response of the dual loop controller

To further verify the validity of the z-domain method in designing the dual loop controller, the controller is simulated with an input reference voltage of 800 V. Figure 5.32 shows that the dual loop controller is able to regulate a load voltage of 800 V when the load is resistive, valued at 40 Ω. Figure 5.33 shows the inductor current with an average current of 20 A. Moreover, the dual controller is simulated in order to track a step reference voltage. The voltage is stepped up from 6 V to 8 V and the tracking response of the dual loop controller is shown in Figure 5.34. At the occurrence of the step, the dual loop controller enters PWM saturation state before it quickly settles with no error when the PWM switching recommences. The response of the inner current loop when the load is 5 Ω shown in Figure 5.35.

5.6 Summary

In this chapter, two closed loop controllers namely the single loop current controller and dual loop voltage and current controller are designed. Moreover, two models namely the average and the small-signal model are used to design both the single and the dual closed controllers. Simulation results based on the average model in designing both the single and dual closed loop controllers, predict an infinite gain margin for both controllers albeit practical systems have a finite gain margin. Nonetheless, simulations results based on the small-signal model in designing both the single and dual closed loop controllers, predict a finite gain margin for both controllers. The small-signal model, closely approximates the gain margins of both controllers by implementing the z-domain techniques and the bifurcation diagrams. This however entails that the average model is unreliable in designing controllers for applications where the performance of the controllers is of utmost importance. Nonetheless, the small-signal model, did not have the short comings of the average model.

In this chapter, both the single loop current controller and the dual loop voltage controller are successfully designed. The main objective of this project is to develop and design a system that emulates the characteristics of a photovoltaic module or array. However, an actual photovoltaic module is a current source and therefore the single loop current controller designed using the small-signal model is implemented by the SAE system in order to emulate the characteristics of a photovoltaic module. The practical implementation of the single loop current controller is discussed in Chapter 7.

Chapter 6

SAE system simulation mode analysis

In this chapter the operation of the Solar Array Emulator (SAE) system in simulation mode is discussed. A graphical user interface (GUI) running on the personal computer (PC) is developed and shown in Figure 6.1. The GUI allows the user to specify whether to operate the simulation mode or the emulation mode. The operation of the SAE system in emulation mode will be discussed in greater detail in Chapter 7. Moreover, the GUI executes the two different modes according to the flow diagram in Chapter 3. When running the simulation, the user can define the photovoltaic (PV) module's parameters such as the short circuit current I_{sc}, open circuit voltage V_{oc} and the number of cells. In addition, the manufacturers of PV modules provide such parameter details in a datasheet of the respective module. Moreover the user can define the module's operating environmental conditions e.g. the ambient temperature, irradiance levels and the percentage shading or percentage uniform accumulation of dust on the module. If the user intends to simulate an array, the number of modules in series and in parallel can also be defined on the GUI. The user can also specify to simulate the effects of utilising the bypass and blocking diodes on the I-V and P-V characteristic curves. The equations derived in Chapter 2 are used by the developed algorithm running on the PC to interpret the user-defined specifications in order to simulate and plot the corresponding characteristic curves.

In this chapter, simulations that can be performed are presented. The simulations are carried out in order to investigate and analyse the non-linear output characteristics of PV modules when exposed to different operating conditions. This simulation process is an intermediate step between designing a module and its mass production. Therefore, this means that the concept can be applied by PV module manufactures for parameter setting of modules to suit specific operation standards during prototyping phase. Furthermore, the concept can also be employed to estimate an array's output power at different operating conditions before the array is installed on site.

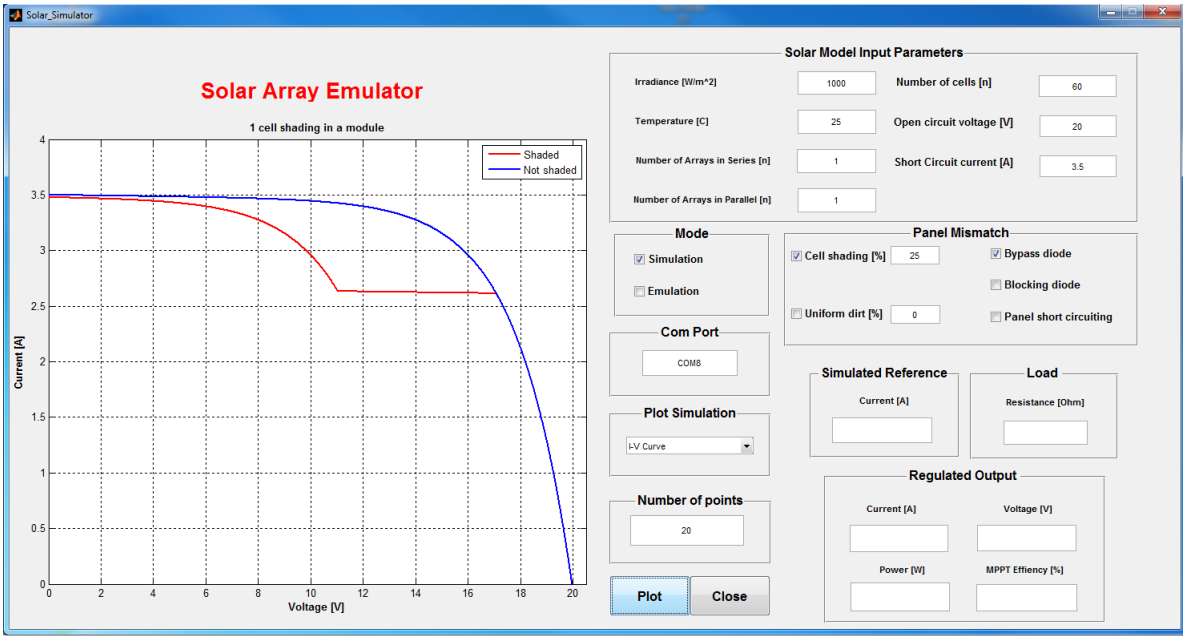

Figure 6.1: Graphical User Interface (GUI) running in simulation mode

6.1 Simulations analysis

In the following sections, different characteristics that affect the overall performance of a PV module or array are analysed through simulation results. Moreover, the use of bypass and blocking diodes for improving module output power efficiency is shading conditions, are analysed. The module in Figure 6.2 with parameters in Table 6.1 are used to simulate the different effects.

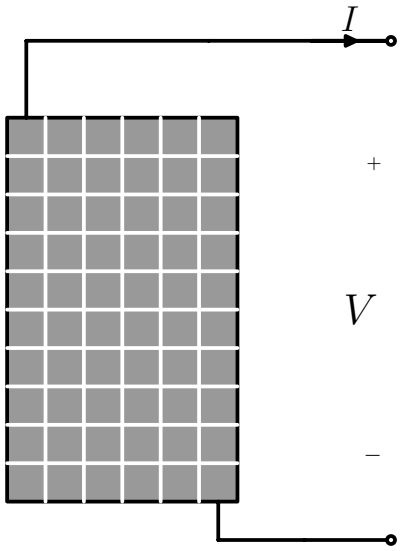

Figure 6.2: Photovoltaic module

Table 6.1: PV module parameters

Open circuit voltage(V_{oc})	20 V
Short circuit current I_{sc}	3.5 A
Number of cells (N_c)	60
Series resistance (R_s)	0.2 Ω
Parallel resistance (R_p)	120 Ω

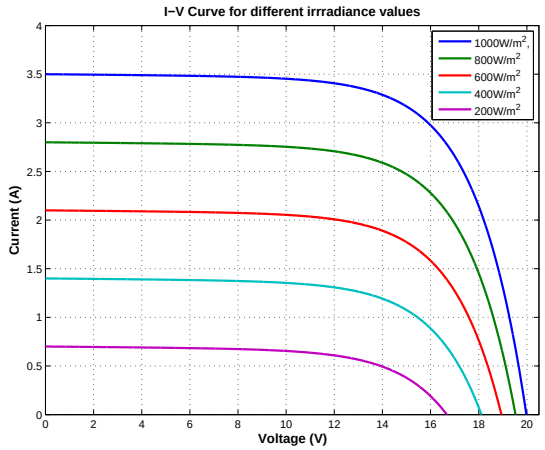

Figure 6.3: Effect of changing irradiation on I-V curve

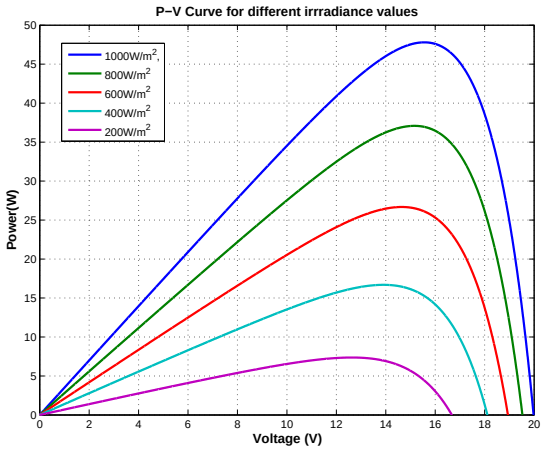

Figure 6.4: Effect of changing irradiation on P-V curve

6.2 Effect of irradiation change on the I-V and P-V characteristic curves

As the irradiation changes, the short circuit current I_{sc} changes in direct proportion as discussed in Chapter 2. The change in I_{sc} with a change in irradiation is described by Equation 2.3.3 in Chapter 2. The module in Figure 6.2 with parameters as in Table 6.1 is used to simulate the effect of changes in irradiance levels. The simulated I-V and P-V characteristic curve for a change in irradiance from $1000\,\mathrm{W\,m^{-2}}$ to $200\,\mathrm{W\,m^{-2}}$ are shown in Figure 6.3 and Figure 6.4. The simulation is carried out at a constant cell temperature of 25 °C. Figure 6.3 indicates that the entire I-V curve shifts downward as the irradiation drops which causes a modest reduction in open circuit voltage V_{oc} as well. Moreover, the maximum power point drops significantly with a drop in irradiation, as depicted in Figure 6.4.

6.3 Effect of cell temperature changes on I-V and P-V curves

The change in cell temperature affects the efficiency of photovoltaic systems, as previously discussed in Chapter 2. The I-V characteristic curve of the module in Figure 6.2 with parameters as in Table 6.1 is used to simulate at a constant irradiance level of $1000\,\mathrm{W\,m^{-2}}$ and varying cell temperature T_{cell} conditions i.e. from 25 °C to 85 °C. The relationship between T_{cell} and V_{oc} is given by Equation 2.3.3. Furthermore, the relationship between T_{cell} and I_{sc} is given by Equation 2.3.4. Figure 6.5 shows that the increase in the module's cell temperature at constant irradiation causes the open circuit voltage V_{oc} to drop by a

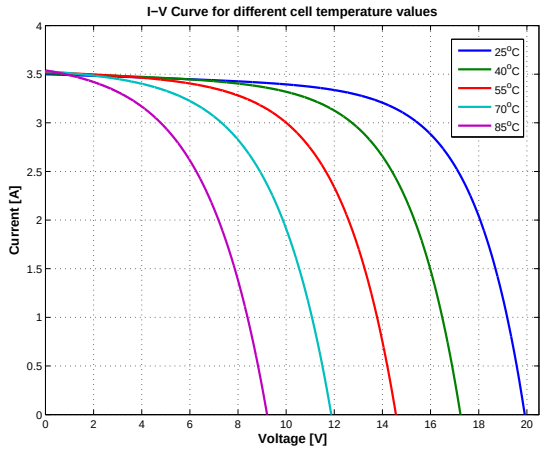

Figure 6.5: Effect of temperature change on the I-V characteristic curve

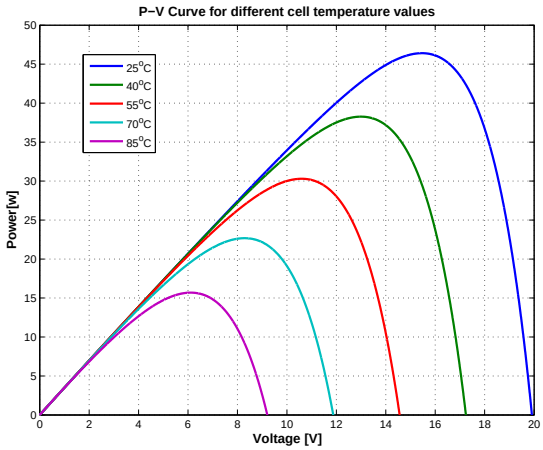

Figure 6.6: Effect of temperature change on the P-V characteristic curve

considerable amount while the short circuit current I_{sc} slightly increases. This verifies the fact that PV modules, surprisingly, do perform better on cold, clear days than on much warmer days. The decrease in voltage also decreases the maximum power generated by the module and thereby reduces the output power efficiency, as illustrated in Figure 6.6.

6.4 Effect of shading on I-V and P-V curves

As previously discussed in Section 2.3.2, PV modules have cells that are series-connected and series mismatches are commonly encountered when one cell is shaded. Therefore PV modules succumb to what is known as mismatch losses caused by the interconnection of cells that do not have identical properties or which experience different operating conditions. The most affected cell undermines the overall performance of the entire module [37]. Moreover, a module can experience uniform sun blockage when it is evenly soiled on its top surface or due to shading caused by a tree. In this section the effects of uniform sun-blockage and mismatch caused by one cell shading are simulated and analysed.

6.4.1 Effect of uniform sun-blockage

The module in Figure 6.2 with parameters in Table 6.1 is simulated in order to analyse the effect of uniform sun-blockage caused by even soiling at a constant temperature of 25 °C. Figure 6.7 shows the I-V curve of a non-soiled module and the I-V curve of a 10% evenly soiled module. When the module is evenly soiled, the I-V curve shifts downward, a response that is similar to the event when the solar intensity is slightly reduced, as can

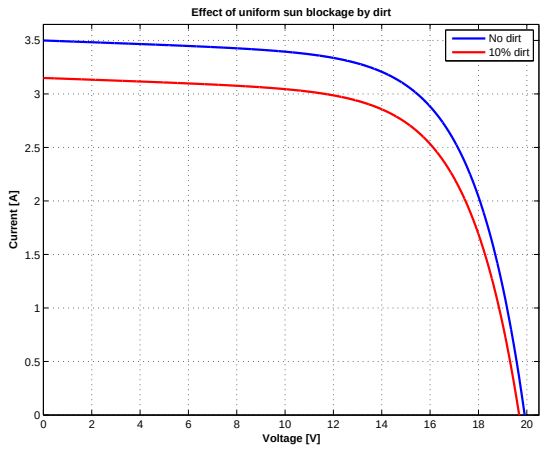

Figure 6.7: Effect of uniform sun-blockage on the module's I-V curve

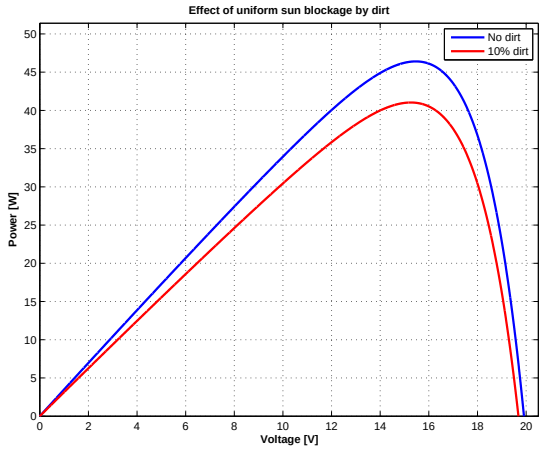

Figure 6.8: Effect of uniform sun-blockage on the module's P-V curve

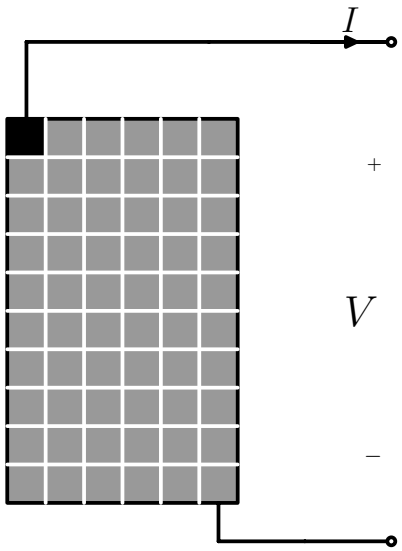

Figure 6.9: One-cell shaded module

be observed in Figure 6.7. Moreover, when the module is evenly soiled, it experiences a 10% loss in power output as shown in Figure 6.8.

6.4.2 Effect of mismatch caused by one-cell shading of a module

The module in Figure 6.9 is simulated at a constant cell temperature of 25 °C and constant irradiation of 1000 W m^{-2} and at different percentages of the area of the cell that is shaded. As previously discussed in Chapter 2, the shaded cell causes a series mismatch that results in the current of the entire module falling to the level of the shaded cell. The current-voltage relationship for a one-cell shaded module is derived in Section 2.3.2.1. From Figure 6.10 it can be observed that as the percentage area of the shaded cell increases,

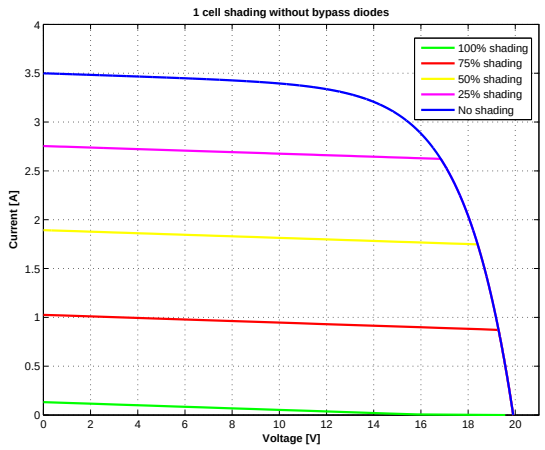

Figure 6.10: Effect of one-cell shading on the module's I-V curve

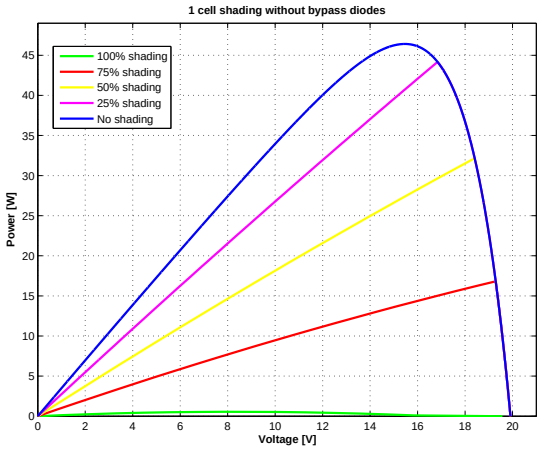

Figure 6.11: Effect of one-cell shading on the module's P-V curve

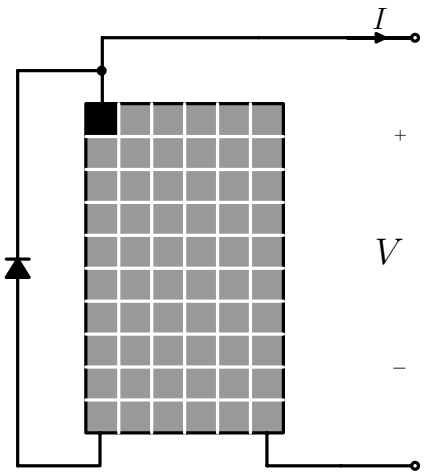

Figure 6.12: One-cell shaded module with bypass diodes

the current of the entire module decreases. Moreover, the maximum power produced falls drastically with increasing percentage area of the cell that is shaded, as shown in Figure 6.11.

The effect of cell shading can be mitigated by the use of a bypass diode, as previously discussed in Section 2.3.2.2. Figure 6.12 shows a one-cell shaded module with a bypass diode that is connected across every 10 cells. By using the bypass diode, the voltage across the shaded cell is equal to the forward bias voltage of the other series cells that share the same bypass diode plus the voltage of the bypass diode. This module with parameters as in Table 6.1 is simulated at a constant cell temperature of 25 °C, a constant irradiation of 1000 W m^{-2} and at different percentages of the area of the cell that is shaded. The voltage across the rest of the cells that are unshaded depends on the percentage of the area of the cell that is shaded, as can be observed in Figure 6.13. Figure 6.14 shows that

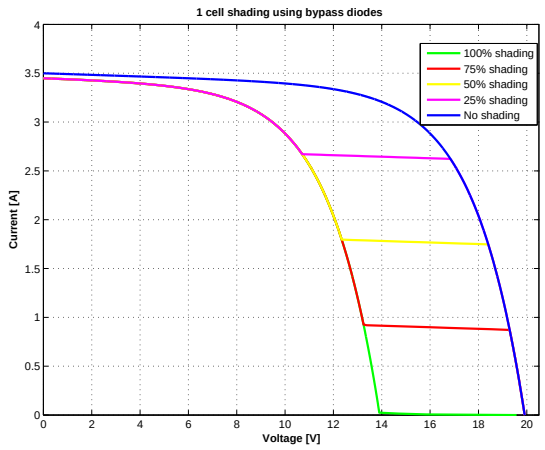

Figure 6.13: Effect of using bypass diodes on the I-V curve of a one-cell shaded module

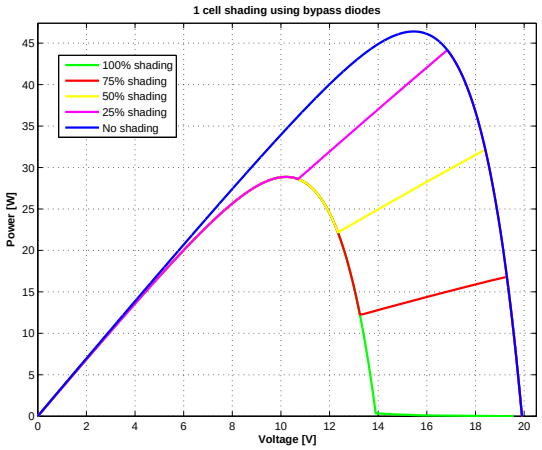

Figure 6.14: Effect of using bypass diodes on the P-V curve of a one-cell shaded module

the power output of a module that implements bypass diodes is improved compared to Figure 6.11, where the simulated module does not implement bypass diodes.

6.4.3 Effect of mismatch due to one-cell shading in a 2-module series-connected array

The 2-module series-connected array in Figure 6.15 is one-cell shaded and employs bypass diodes in order to improve the overall performance of the array. Each module in the array configuration has parameters shown in Table 6.1. The array is simulated at a constant cell temperature of 25 °C, a constant irradiation of 1000 $\mathrm{W\,m^{-2}}$ and at different percentages of the area of the cell that is shaded. The current flowing in both modules is the same and the voltage across the unshaded cells depends on the percentage of the area of the cell that is shaded, as can be observed in Figure 6.16. The maximum power output changes with the change in the percentage degree of cell shading, as shown in Figure 6.17.

6.4.4 Effect of mismatch due to one-cell shading in an array with 2-modules connected in parallel

Figure 6.18 shows a one-cell shaded module in parallel with a module with unshaded cells. The array makes use of a bypass diodes. The shaded cell causes a voltage drop across the module to which it is connected and this results in a voltage mismatch between the one-cell shaded module and the module with unshaded cells. This results in an imbalance between the parallel connected modules as one module has a high voltage than the other. A blocking diode, discussed in greater detail in Section 2.3.2.2 is used and connected in

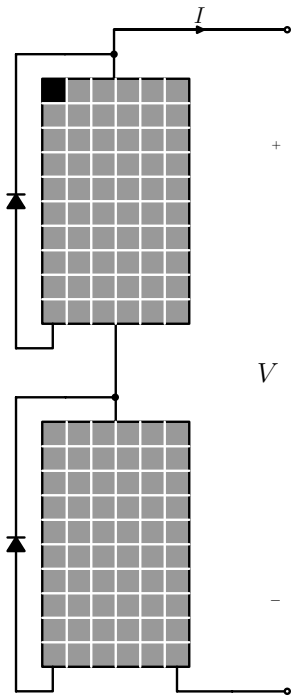

Figure 6.15: One-cell shaded series-connected 2-module array

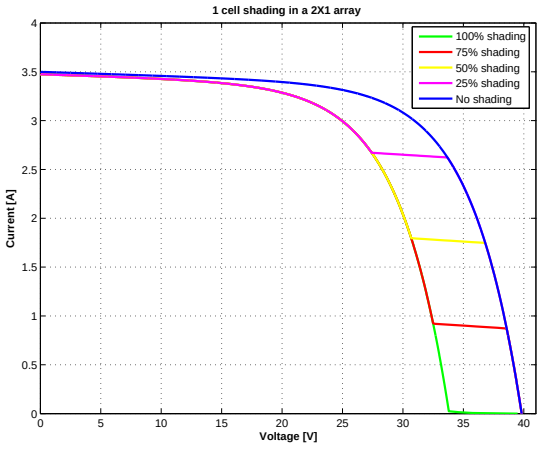

Figure 6.16: Effect of one-cell shading on the I-V curve of a series-connected 2-module array

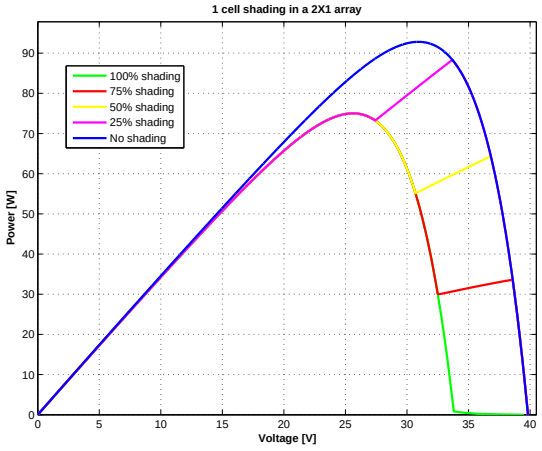

Figure 6.17: Effect of one-cell shading on the P-V curve of a series-connected 2-module array

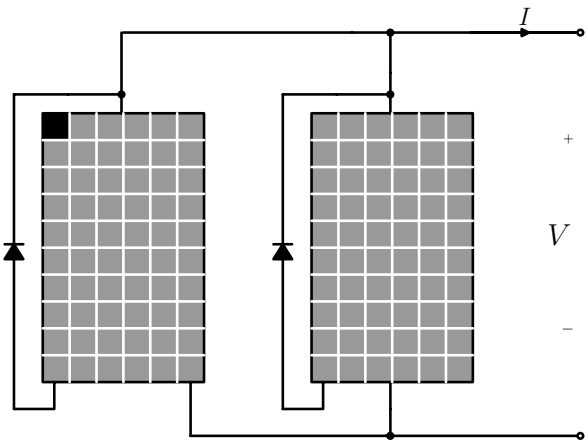

Figure 6.18: Array without blocking diodes

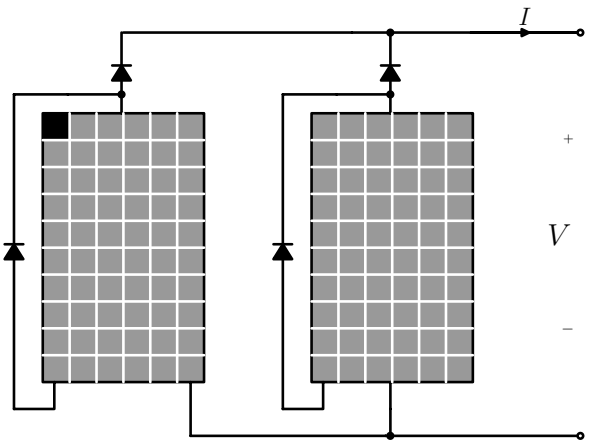

Figure 6.19: Array with blocking diodes

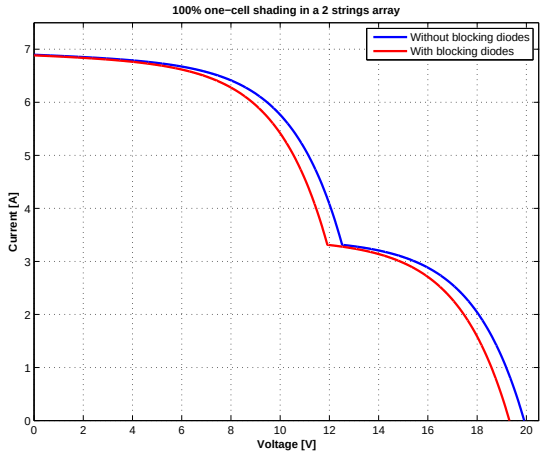

Figure 6.20: Effect of one-cell shading on the I-V curve of a 2-strings array

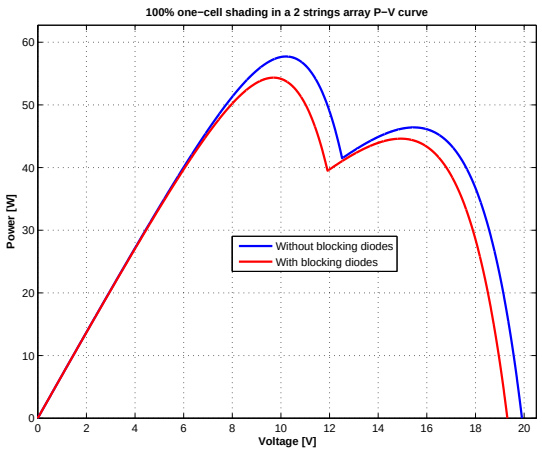

Figure 6.21: Effect of one-cell shading on the P-V curve of a 2-strings array

series with each module in the array as shown in Figure 6.19. The function of the blocking diode is to prevent reverse current flowing into the one-cell shaded module. Both arrays are simulated at a constant cell temperature of 25 °C, a constant irradiation of 1000 W m^{-2} and with 100% area of the cell shaded. Figure 6.20 shows the I-V characteristic curves of the simulated array without blocking diodes and the array with blocking diodes. The array with blocking diodes experiences a small drop in voltage due to the blocking diodes. Figure 6.21 shows the resulting P-V characteristic curves for both arrays indicating a slight reduction in power generated by an array with blocking diodes.

6.4.5 Effect of mismatch caused by one-cell shading in a 2-strings of 40-modules each array

The array shown in Figure 6.22 is connected in a 2 strings of 40 modules each array. The structure is one-cell shaded and employs blocking and bypass diodes. Each module has parameters as shown in Table 6.1 and the array is simulated at a constant cell temperature of 25 °C, a constant irradiation of 1000 W m^{-2} and at different percentages of the area of the cell that is shaded. As previously mentioned, the voltage across the string with the shaded cell, depends on the percentage of the area of the cell that is shaded. A voltage mismatch occurs as both strings are generating different voltages when measured independently creating an imbalance. Moreover a voltage drop is experienced across each string due to the blocking diodes. However, the voltage drop is small relative to the voltage across the whole array, hence there is no significant impact on the I-V and P-V characteristic curve. The resulting I-V characteristic curve is shown in Figure 6.23 and the resulting P-V characteristic curve is shown in Figure 6.24.

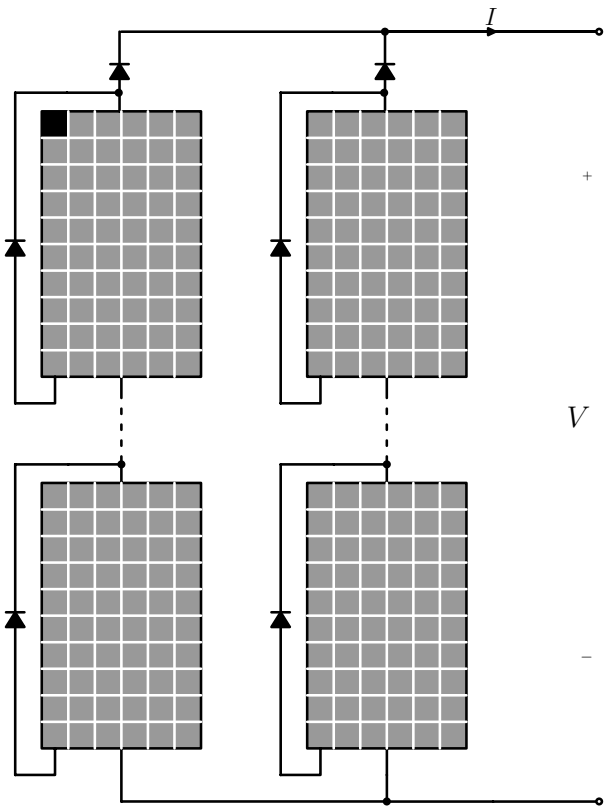

Figure 6.22: One-cell shaded 2-strings, 40-module each array with blocking diodes

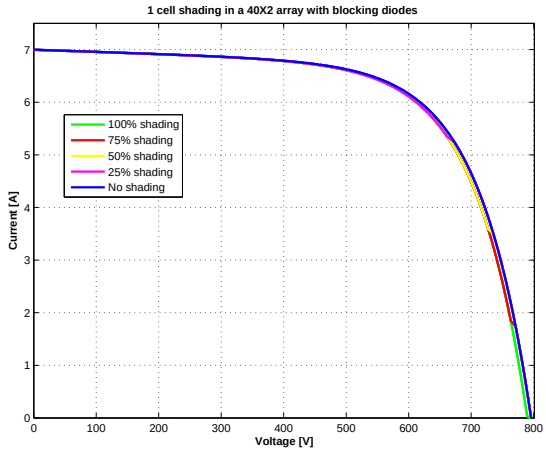

Figure 6.23: Effect of one-cell shading on the I-V curve of a 2-strings, 40-modules each array

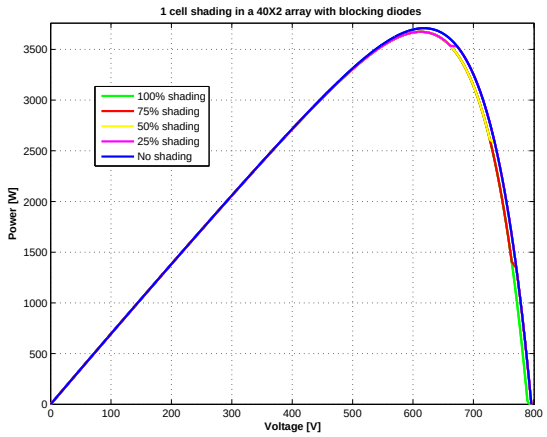

Figure 6.24: Effect of one-cell shading on the P-V curve of a 2-strings, 40-modules each array

6.5 Effect of mismatch of caused by a shorted module in a 5-string, 45-modules each array

Figure 6.25 shows a 5-string, 45-modules each array that has one of its modules short circuited. Each module in the array has parameters as shown in Table 6.1 and the array is simulated at a constant cell temperature of 25 °C and a constant irradiation of 1000 W m^{-2}. Module short circuiting can be as a result of the module being completely shaded or broken down. The breakdown can be due to insulation degradation with weathering, resulting in cracking and corrosion. The shorted module causes a voltage drop across the string to which it is connected, resulting in a voltage mismatch occurring due to the affected string generating a different voltage to the rest of the strings. The simulated I-V curves Figure 6.26, shows the difference in characteristics between the array without a shorted module and the array with a shorted module. The resulting P-V curves are shown in Figure 6.27.

6.6 Summary

In this chapter, the SAE system is operated in the simulation mode in order to simulate the effects of temperature change, irradiation change, shading and module shorting on the I-V and P-V characteristic curves of different array configurations. A user friendly GUI is developed that allows the user to define the module parameters, array configurations and operating conditions. The effects of employing bypass and blocking diodes for improving the performance of different array configurations are also analysed.

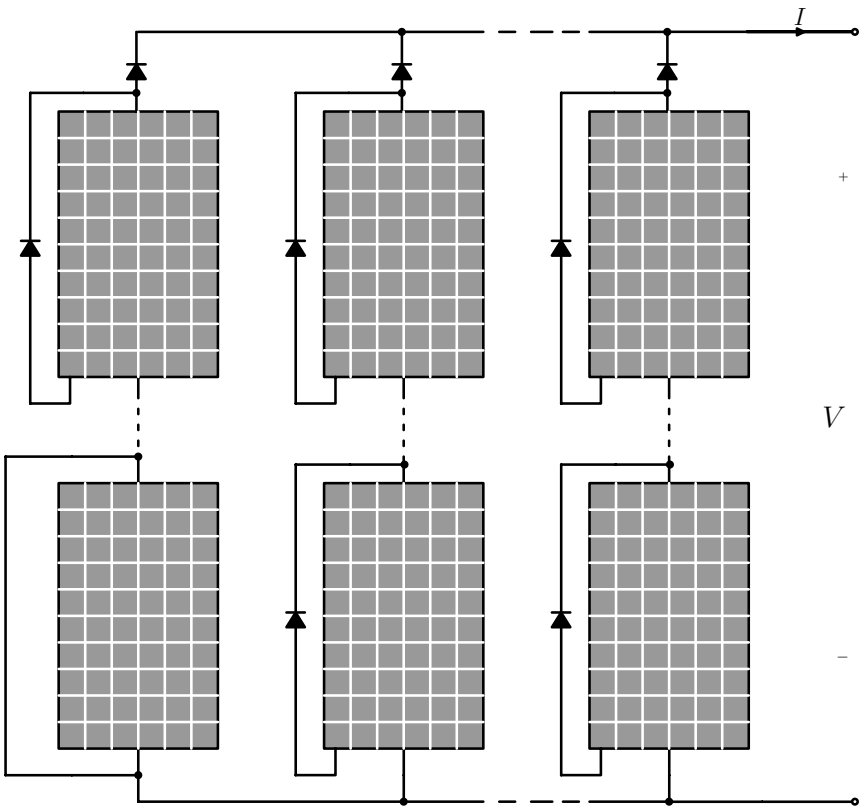

Figure 6.25: 45 X 5 modular array with one module shorted

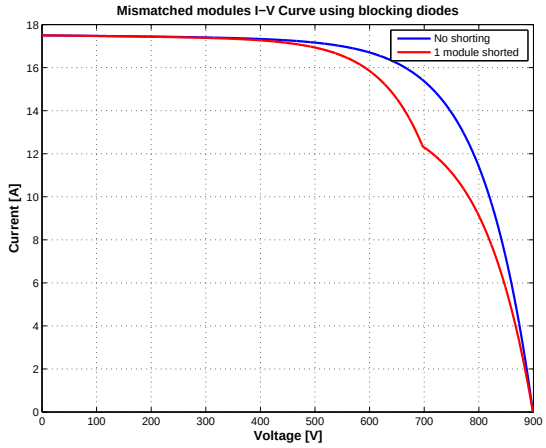

Figure 6.26: Effect of module shorting on the I-V curve of a 5-string, 45-modules each array

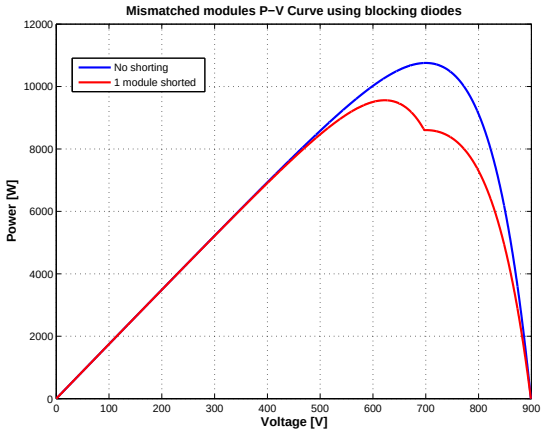

Figure 6.27: Effect of module shorting on the P-V curve of a 5-string, 45-modules each array

Chapter 7

SAE system practical tests

In this chapter the Solar Array Emulator (SAE) system emulates the non-linear output characteristics of an actual photovoltaic (PV) module. It is used as a technological system that evaluates the performance of PV power electronics systems such as a grid-tie inverter and a maximum power point tracking (MPPT) active load. The SAE system is rated at 20 kW with maximum current of 18 A and a maximum voltage of 900 V and therefore the system is designed to emulate any array with a maximum current and a voltage that falls within the specified limits. A graphical user interface (GUI) running on a personal computer (PC), shown in Figure 7.1 is designed to allow the user to define the PV module's operating environmental conditions, degree of partial shading and the module's parameters. If the user intends to emulate an array, the user can specify the number of modules in parallel and in series. In addition, on the GUI, the user can specify if the module or array makes use of blocking or bypass diodes. The GUI in Figure 7.1 is operated in emulation mode and remember that in Chapter 6, the GUI is operated in simulation mode. The GUI has the advantage of displaying the emulation process on the axes available. The current controller implemented by the SAE system for current regulation is designed in Chapter 5. The hardware setup of the SAE system is shown in Figure 7.2. The hardware system is interfaced with the GUI via a serial communication port. The experiments conducted in this chapter include:

1. The SAE system connected to a variable resistor in order to test the system's experimental performance in emulating a PV array under changing load conditions.

2. The SAE system connected to an MPPT active load in order to evaluate its maximum power point tracking mechanism under different operating conditions.

3. The SAE is connected to a grid-tie inverter in order to evaluate the mechanism the inverter employs in delivering power from the PV module to the grid.

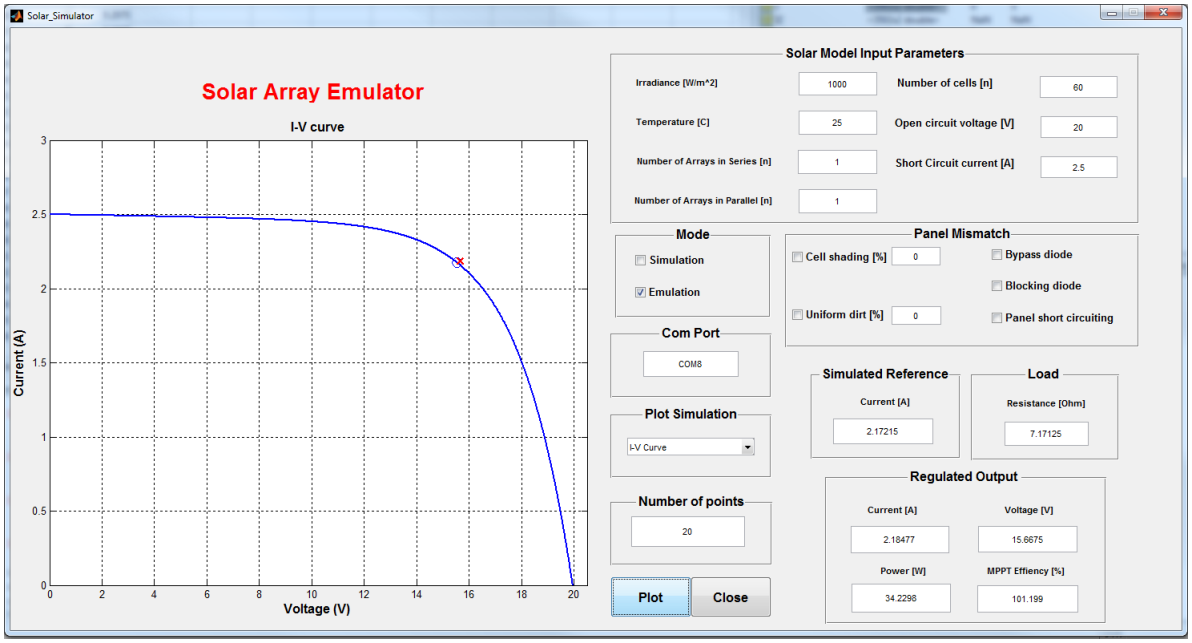

Figure 7.1: Graphical user interface (GUI) running in emulation mode

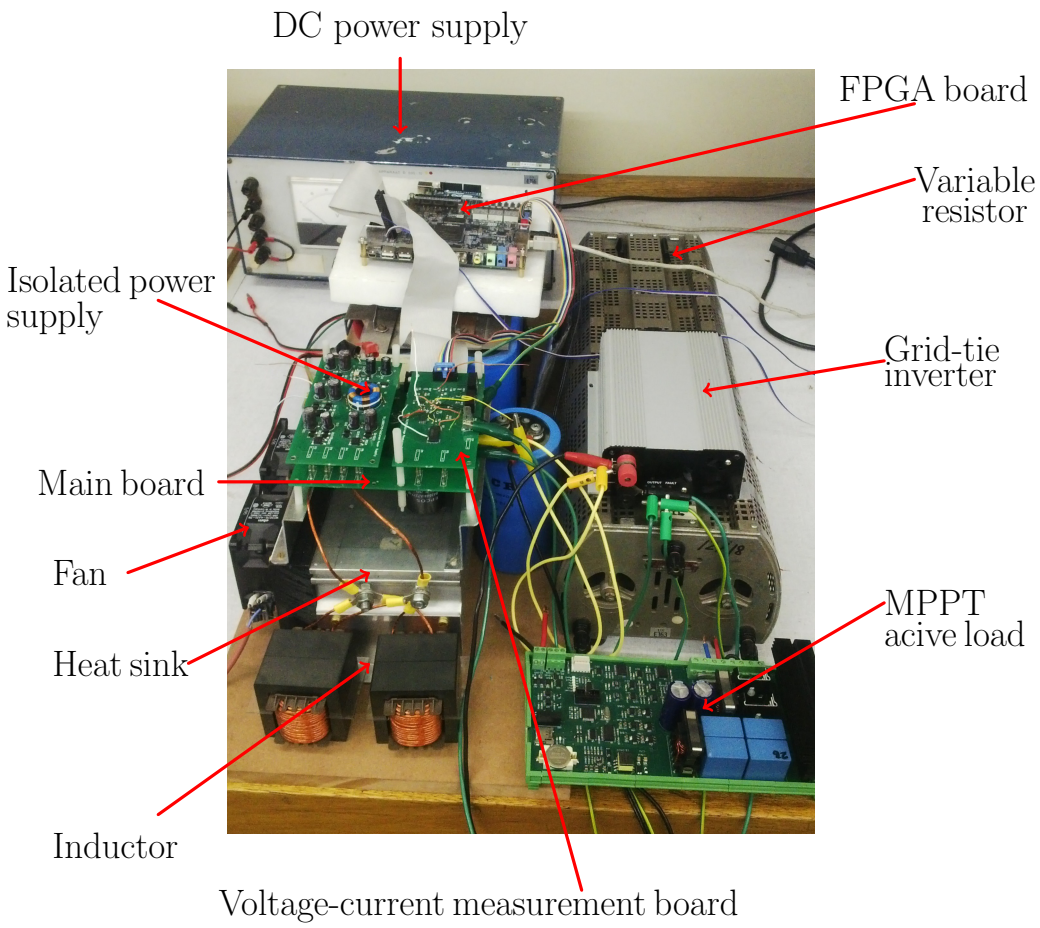

Figure 7.2: The hardware set up of the SAE system

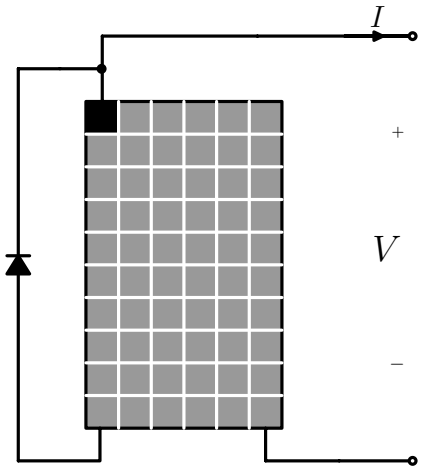

Figure 7.3: One-cell shaded module with a bypass diode

Table 7.1: PV module parameters

Open circuit voltage (V_{oc})	20 V
Short circuit current (I_{sc})	2.5 A
Number of cells (N_s)	60
Series resistance (R_s)	0.0221 Ω
Shunt resistance (R_p)	125 Ω

The module to be emulated by the SAE system is shown in Figure 7.3. Different array configurations using this module and it parameters in Table 7.1, are considered for the experimental tests in this chapter.

7.1 SAE system connected to variable resistor

In this section the SAE system is tested for its experimental performance i.e. steady and dynamic response when connected to a variable resistor. The SAE emulates the non-linear output characteristics of two modules connected in parallel to each other. In addition, one of the modules has a cell that has 25% of its area shaded. The operating environmental conditions are a temperature of 25 °C and irradiation of 1000 W m^{-2}.

7.1.1 Steady state analysis

According to the user defined specifications described above, the SAE system emulates the theoretical I-V curve shown in Figure 7.4. Moreover, Figure 7.4 shows the experimental steady-state performance of the proposed SAE system as the load is changed. The corresponding measured P-V operating points are shown in Figure 7.4. The measured operating points of the SAE system as the load is changed, closely approximate the theoretical I-V curve being emulated as shown in Figure 7.4 . In order to evaluate the accuracy of the SAE system in emulating the theoretical I-V curve, the percentage deviation is calculated using Equation 7.1.1, whereby $X_{theoretical}$ is the theoretical operating point and $X_{measured}$ is the measured operating point.

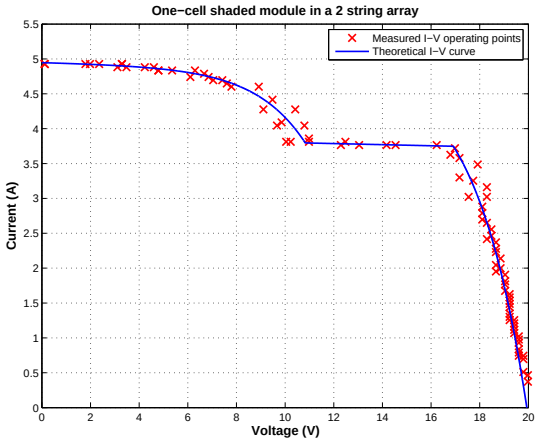

Figure 7.4: Experimental I-V operating points as the load resistance is varied

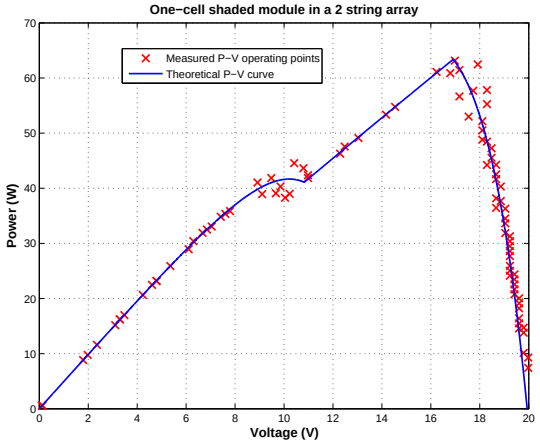

Figure 7.5: Experimental P-V operating points as the load resistance is varied

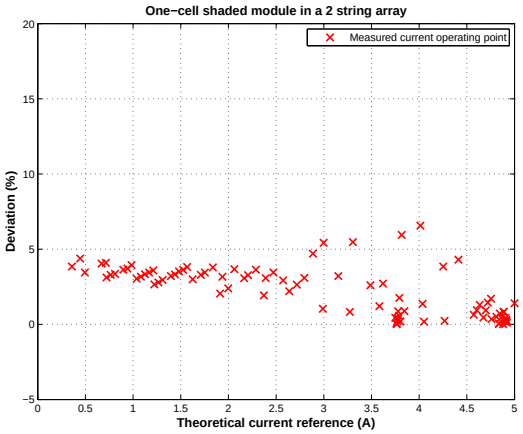

Figure 7.6: Current percentage deviation from the reference current at each sampling point

$$\epsilon(\%) = \frac{|X_{theoretical} - X_{measured}|}{X_{theoretical}} \tag{7.1.1}$$

The SAE system regulates a new reference current at every sampling point i.e. whenever the load line changes. Figure 7.6 shows percentage deviation of the measured current from the theoretical reference current at each sampling point. An average percentage deviation of 3.5% is observed, according to Figure 7.6. The percentage deviation of the measured values from the theoretical values is attributed to a number of factors. Chief amongst them is the effect of switching noises on the reference voltage of the analog to digital (A/D) converter. The switching noise influences the integrity of the A/D converter measured values as previously discussed in Chapter 3. However, the measured results shown in Figure 7.4 indicate that the SAE system closely approximates the steady state

characteristics of an actual PV array.

7.1.2 Dynamic response of the SAE system

The experimental dynamic response time of the SAE system is tested for a step change in the load resistance. A switch is used to instantly change load resistance, thus changing the operating points on the I-V characteristic curve being emulated by the SAE system. Figure 7.7 shows the dynamic response of the SAE system when the load changes the operating point from 14.91 V and 4.54 A to 18.94 V and 2.78 A. The system takes approximately 25 ms to arrive at the desired working point. The dynamic response is tested for different situations and the dynamic response always lasts for less that 25 ms. In order for the SAE system to accurately emulate an actual PV module or array, it should have a dynamic response time less than that of the PV power electronic system being evaluated, in this case the MPPT active load and the grid-tie inverter. This is necessary so that the SAE system does not influence the dynamic performance of the system under evaluation. In the following sections the SAE system is implemented in evaluating the steady state performance of the MPPT active load and the grid-tie inverter under different operating conditions.

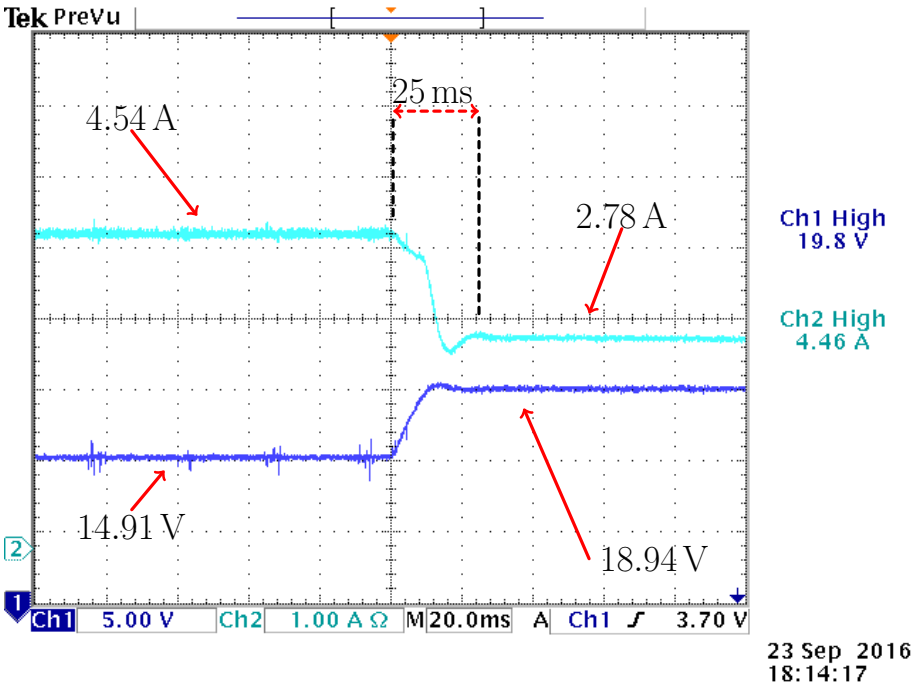

Figure 7.7: Dynamic response of the SAE system when the load is changed

7.2 SAE system connected to MPPT active load

In this section the MPPT active load is evaluated by the SAE system. The MPPT active load is an intelligent power electronic system that operates at the maximum power point of an array at any given time and dumps the power in a dumping resistor. The system is designed and developed in [38] and it employs a Perturb and Observe technique for maximum power point tracking. The system has specifications shown in Table 7.2.

Table 7.2: MPPT active load specifications

Maximum Input Voltage (V_{in})	100 V or 50 V
Maximum Input Current (I_{in})	5A/100V or 10A/50V
Switching frequency (f_s)	40 kHz
Dumping resistor (R)	1 Ω, 350 W

7.2.1 Steady state analysis of the MPPT active load

The SAE system emulates the module in Figure 7.3, operating at a temperature of 25 °C, irradiation of 1000 W m^{-2}. The emulated module has a cell that has 25% of its area shaded. Figure 7.8 shows the theoretical I-V profile emulated and the measured I-V operating points of the MPPT actve load. Figure 7.8 shows the corresponding theoretical P-V curve and the measured P-V operating points. Figure 7.8 shows that the MPPT active load tracks the maximum power point accurately. The percentage deviation of the measured power from the theoretical maximum power point is calculated using Equation 7.1.1. Figure 7.10 shows the percentage deviation measured power from theoretical maximum power point. The average percentage deviation is observed as approximately 5% based on Figure 7.10.

Another experiment is conducted in order to evaluate the effect of irradiation change on the steady state performance of the MPPT active load. An array configuration two modules in parallel, operating at a temperature of 25 °C is emulated by the SAE system. Each PV module has parameters shown in Table 7.1. The operating irradiance level is increased from 800 W m^{-2} to 1000 W m^{-2}. Figure 7.11 shows the theoretical I-V characteristic curve and the measured I-V operating points of the MPPT active load. It is observed from Figure 7.11 that the MPPT active load operates close to the theoretical maximum power point. It is observed from Figure 7.13 that the average percentage deviation of the measured power from the maximum power point at irradiance level of 800 W m^{-2}, is approximately 1.2. Moreover, in Figure 7.14 it is observed that average percentage deviation of the measured power is approximately 1.5% when the SAE system is emulating the PV array at an irradaince level of 1000 W m^{-2}. As previously mentioned

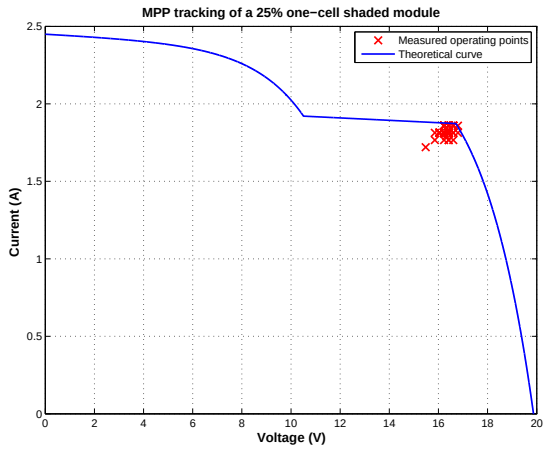

Figure 7.8: Measured I-V operating points on the maximum power point of the SAE system

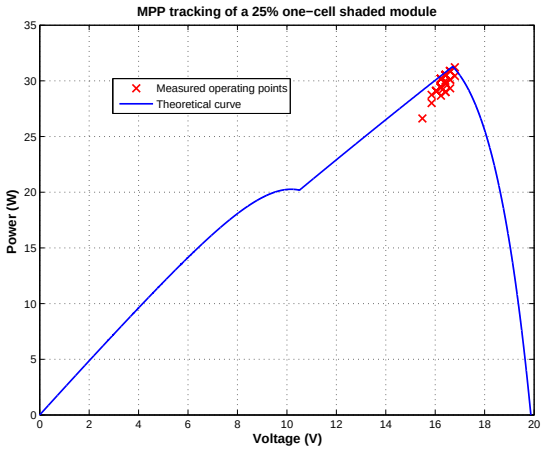

Figure 7.9: Corresponding P-V operating points on the maximum power point of the SAE system

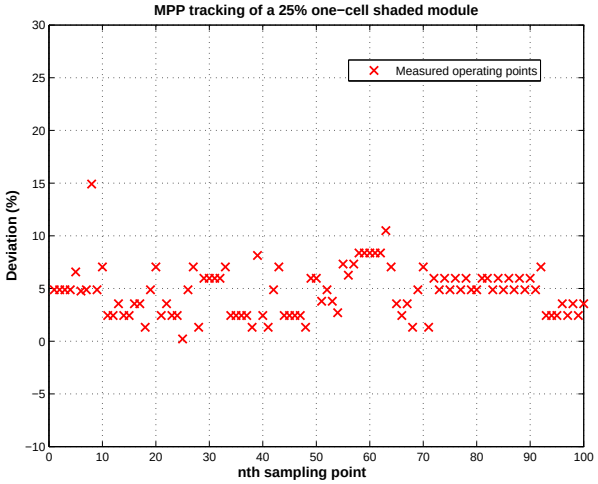

Figure 7.10: Measure of deviation of the measured power from the theoretical maximum power point

the effect of switching noise on the A/D converter results in the measured operating points deviating from the theoretical I-V profile being emulated by the SAE system. Moreover, the algorithm implemented by the MPPT active load searches for the maximum power point constantly by adjusting its duty cycle and therefore the measured operating points oscillates around the theoretical maximum power point.

7.3 SAE system connected to the Grid-tie inverter

The grid-tie inverter implements a Voltage Constant technique to deliver as much power as possible from the PV array to the grid. The inverter specifications are illustrated in

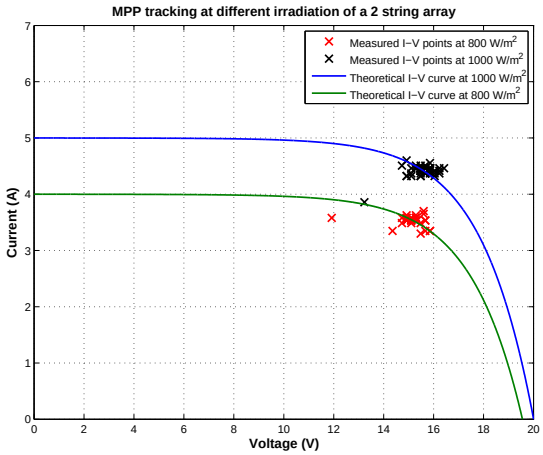

Figure 7.11: I-V operating points of the MPPT active load under different irradiance level conditions

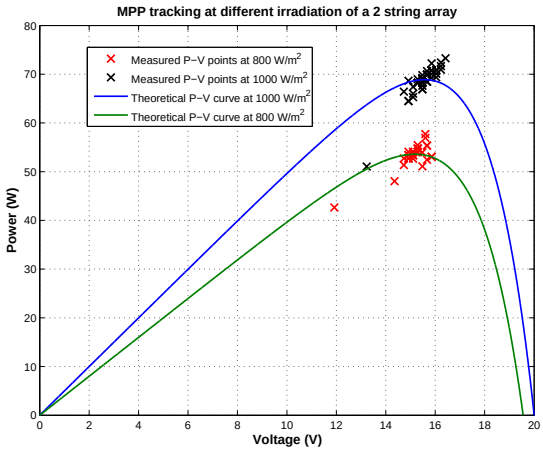

Figure 7.12: P-V operating points of the MPPT active load under different irradiance level conditions

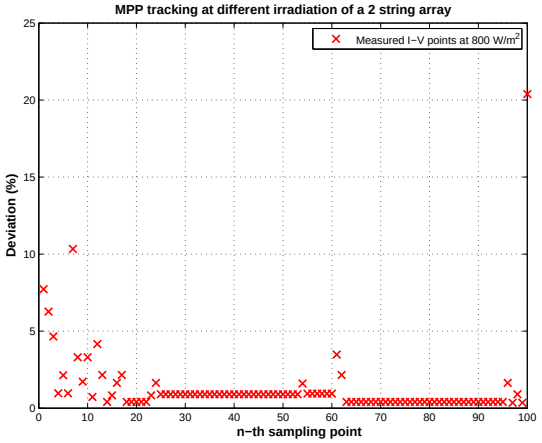

Figure 7.13: Deviation of measured operating power points from theoretical MPP at irradiance level of 800 W m^{-2}

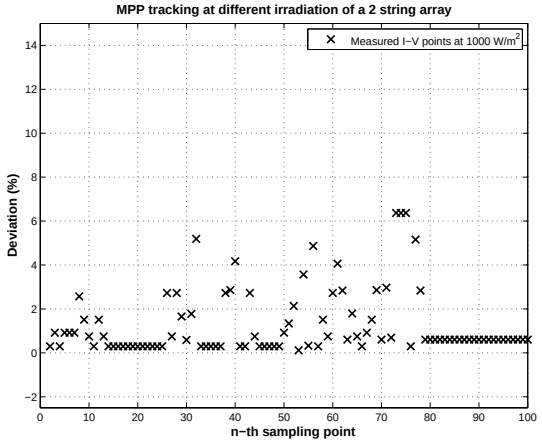

Figure 7.14: Deviation of measured operating power points from theoretical MPP at irradiance level of 1000 W m^{-2}

Table 7.3. In this section, the experimental performance evaluation of the grid-tie inverter is evaluated.

Table 7.3: Grid-tie inverter specifications

Normal AC output power	225 W
Maximum AC output power	250 W
AC Output voltage range	190 V-260 V
AC frequency(f) range	46 Hz - 65 Hz
DC Input voltage(V_s)	10.8 V - 30 V
Operating temperature range	−10 °C - 45 °C
Stackable	Yes

7.3.1 Steady state performance analysis of the Grid-tie inverter

The module in Figure 7.3 operating at a temperature of 25 °C, irradiation of 1000 W m^{-2} and at 0% one-cell partial shading is emulated by the SAE system connected to the grid-tie inverter. Figure 7.15 shows the steady state I-V operating points of the grid-tie inverter and the corresponding P-V operating points are shown in Figure 7.16. The Voltage Constant technique employed by the grid-tie inverter, ensures that the inverter operates at approximately 75% to 85% of the open circuit voltage. From Figure 7.15 it is observed that the inverter regulates approximately 17 V at its input, which is 85% of the module's open circuit voltage. This verifies the Voltage constant technique employed by the grid-tie inverter. Measured current and voltage operating points are observed to be deviating away from the theoretical curve being emulated by the SAE system. The deviations are due to the noise introduced by the switching circuits, as previously discussed.

Another experiment is conducted in order to evaluate the performance of the grid-tie inverter where the SAE system emulates an array with two modules connected in parallel. The operating temperature of 25 °C and the irradiance level change from 1000 W m^{-2} to 200 W m^{-2}, are considered. When the SAE system is emulating the I-V characteristics of the array operating at an irradiance level of 1000 W m^{-2}, the grid-tie inverter regulates approximately 17 V at its input, which is 85% of the emulated PV array. However, when the irradiance level is dropped to 200 W m^{-2}, the grid-tie inverter regulates approximately 16.8 V at its input regardless of change of the PV array open circuit voltage due to drop in irradiance level, as shown in Figure 7.17. Figure 7.18 shows the corresponding P-V operating points of the grid-tie inverter. It can be observed from Figure 7.18 that the grid-tie inverter does not operate at the maximum power point of the emulated PV array.

7.4 Summary

The SAE system is tested for evaluating the steady state performance of photovoltaic power electronic systems namely the grid-tie inverter and the MPPT active load. The dynamic response time of the SAE system is tested by changing the load resistance instantaneously using a switch and observing the time the system takes to settle at a new operating point. Several tests are conducted and the dynamic response time is always less than 25 ms. When the SAE system is connected to a variable resistor and as the resistance is varied, the measured operating points of the SAE system closely approximate the theoretical I-V characteristic curve being emulated. The average percentage deviation of the measured current from the theoretical I-V characteristic curve is 3.5%.

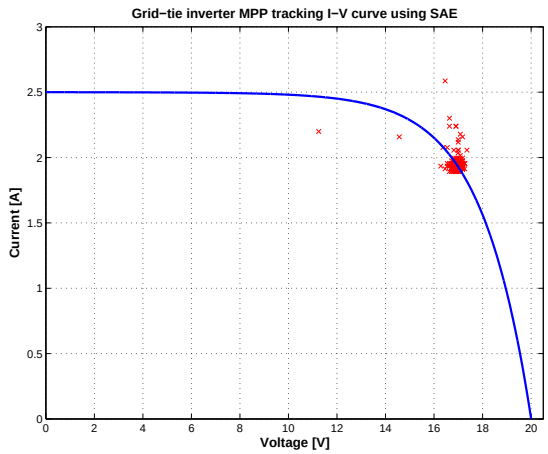

Figure 7.15: I-V operating points of the Grid-tie inverter being evaluated by the SAE system

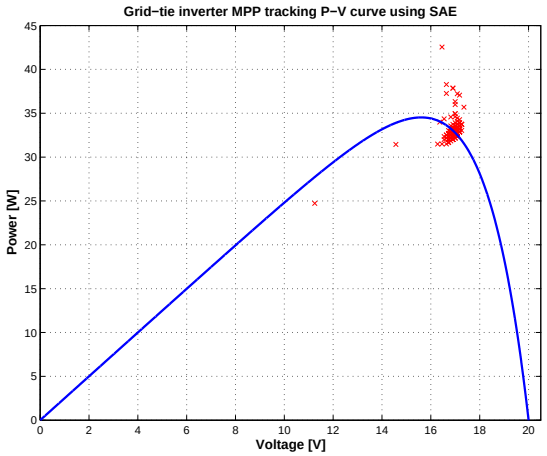

Figure 7.16: Corresponding P-V operating points of the Grid-tie inverter being evaluated by the SAE system

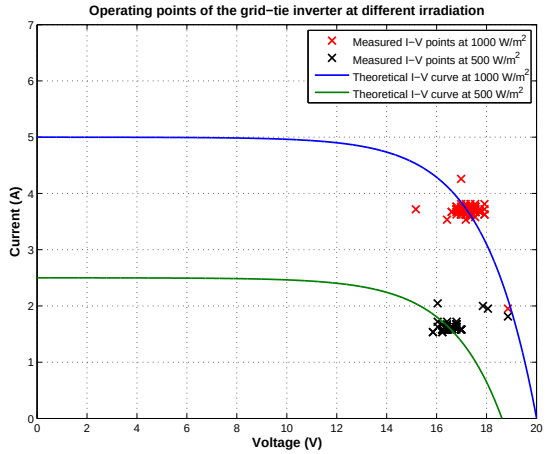

Figure 7.17: I-V operating points of the Grid-tie inverter under different irradiance level conditions

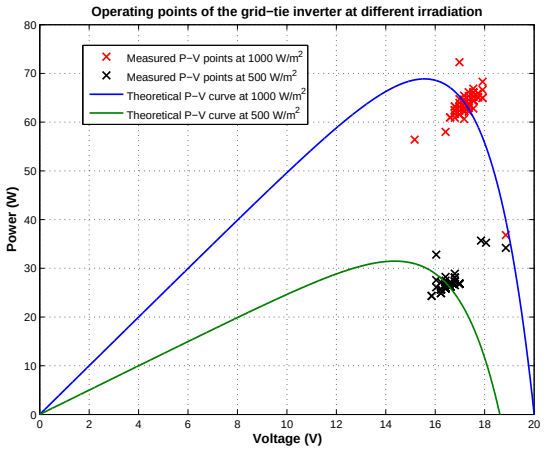

Figure 7.18: Corresponding P-V operating points of the Grid-tie inverter under different irradiance level conditions

The percentage deviation has been attributed to the noise from the switching circuits which affects the integrity of the A/D converter's measured values.

When the MPPT active load is connected to the SAE system, the MPPT active load successfully operates at the MPP of the emulated I-V characteristic curve. The experiment is repeated for a change in irradiance levels and the MPPT active load is able to successfully adjust to the effect of irradiance change and track the new MPP. However the current and voltage operating points slightly deviates from the theoretical MPP and this has been attributed to the effect of noise affecting the integrity of measured values. Furthermore, the performance of the grid-tie inverter is evaluated by the SAE system. The experimental results indicate that the grid-tie inverter regulates approximately 85%

of the open circuit voltage of the emulated PV array. This verifies the Voltage constant technique employed by the grid-tie inverter in delivering power to the grid.

Chapter 8

Solar Array Emulator thesis conclusion

In this chapter, the research findings of each chapter are presented. In addition, recommendations and possible improvements that can be made to the Solar Array Emulator (SAE) system are discussed.

8.1 Research findings

8.1.1 Chapter 1

In this chapter, a brief explanation of the reasons behind growing interest in solar photovoltaic energy is presented. The factors that influence the efficiency and overall performance of solar photovoltaic systems, are briefly described. The motivation and objectives of this thesis are explained.

8.1.2 Chapter 2

Two models that ideally characterises a solar photovoltaic cell are discussed. The effects of environmental conditions such temperature, shading, irradiation on the non-linear output characteristics of a solar photovoltaic module or array, are discussed in greater detail. The equations that characterises the effects of the environmental conditions on the performance of solar photovoltaic modules, are derived. The algorithms implemented by solar photovoltaic power electronics systems such as maximum power point trackers, inverters, battery chargers e.t.c, to deliver power from the source to the load, are also discussed. Existing solutions that evaluate the performance of the photovoltaic power electronic systems under different operating conditions, are presented.

8.1.3 Chapter 3

Detailed explanation on how the Solar Array Emulator system operates is given. The technique employed by the SAE system when operating in emulation mode, is developed. The algorithms responsible serial communication, analog to digital (A/D) conversion are designed through the use of state machines. The accuracy of the A/D converter in measuring current and voltage, is investigated. The operation of the digital PI controller and the pulse width modulator, is illustrated. In addition, the algorithm responsible for including a dead time between the high side and the low side pulse width modulation gate signals, is designed.

8.1.4 Chapter 4

The design strategies of the hardware components of the Solar Array Emulator, are discussed. Equations are derived based on the operation of the synchronous DC/DC converter in order to design for the converter's output filter capacitor, input bus capacitor and inductor. The gate driver circuitry is designed, together with the isolated power supply circuitry. A Sallen-Key low pass filter responsible for filtering any noise after amplification and isolation of signals, is designed. Moreover, the equations to calculate the power losses in the IBGT module used by the DC/DC converter, are derived. The calculated power losses are used to determine a suitable heat-sink for the IGBT module.

8.1.5 Chapter 5

Two closed loop controllers namely the single closed loop current controller and the dual closed loop voltage and current controller, are designed. Two models namely the average model and the small-signal model, are proposed for the design of the two closed loop controllers. A comparison is made between the models based on the ability of each model to accurately predict the stability margins of both closed loop controllers. Simulation results based on the average model predicts an infinite gain margin for both closed loop controllers. However, simulation results based on the small-signal model which employs z domain method, indicates a finite gain margin for both controllers. Moreover, by implementing bifurcation diagrams, the small-signal model predicts gain margins for both closed loop controllers, approximately equal to the gain margins predicted by the z-domain method. Therefore it is concluded that the small-signal model is accurate for implementation in designing closed loop controllers. Therefore the single closed loop current controller and the dual closed loop voltage and current controller are successfully designed using the small-signal model. However, the single closed loop current controller

is implemented by the SAE system for current regulation because a solar photovoltaic module or array are current sources. Hence for the SAE system to accurately emulate a photovoltaic module or array, it must be a current regulator.

8.1.6 Chapter 6

Another functionality of the SAE systems is explored in this chapter. The SAE system is operated in simulation mode in order to evaluate the effects of environmental conditions such as temperature, irradiation and shading on the non-linear output characteristics of a solar photovoltaic module or array. A graphical user interface (GUI) is presented, that allows the user to define the operating environmental conditions, photovoltaic module parameters, and the array configuration to be simulated. Different environmental conditions, different array configurations and the effects of using bypass and blocking diodes are simulated and analysed.

8.1.7 Chapter 7

The operation of the SAE system running in emulation mode is explored. The SAE system successfully emulates the output characteristics of an actual solar module or array at different operating conditions. The SAE system is used to evaluate the steady state performance of the MPPT active load and the experimental results indicate that the MPPT active load is able to operate at the maximum power point of the emulated arrays under different different operating conditions. This validates the algorithm implemented by the MPPT active load for maximum power point tracking. Moreover, the SAE system is used to experimentally evaluate the performance of the grid-tie inverter at different operating conditions. The experimental results indicate that the grid-tie inverter regulates its input voltage at approximately 85% of the open circuit voltage of the emulated module or array. This verifies the Voltage constant technique implemented by the grid-tie inverter to deliver power from the source to the grid.

8.2 Recommendations

8.2.1 Controller design optimisation

It is suggested that other closed loop controller design strategies be investigated in order to further improve the speed of the current controller implemented by he SAE system. The possibility of directly designing closed loop controllers in z-domain, instead of continually

transforming between the s- and the z-domain, should also be investigated. Moreover, the possibility of implementing double-edge, triangular carrier, should also be investigated.

8.2.2 Real time operating conditions

The SAE system can be extended to emulate a solar photovoltaic module or array under real-time environmental conditions. This can be made possible by implementing solar irradiation and temperature sensors.

8.3 General Conclusion

The thesis objectives as set in Section 1.3 have been achieved. All the different sub-systems that makes up the SAE system are successfully designed. Different algorithms implemented by the SAE system are also successful developed. The SAE system has been designed in such a way that it is flexible, controllable, low cost and has high power ratings. The results of the simulation mode and the emulation mode, indicate that the SAE system is an appropriate system that can be used by manufactures or laboratories dedicated to the design and development of solar photovoltaic power systems.

In closing, the course of the project has been quite an enjoyable learning curve. The knowledge and the experience gained is priceless.

Appendices

Appendix A

State space representation of closed loops systems

A.1 Derivation of the state-space representation of the single loop current controller

By analysing the single loop current controller in Figure A.1:

$$V_d P_o = \dot{x_1} + r_L x_1 + x_2 \tag{A.1.1}$$

And

$$x_2 = R(x_1 - C\dot{x_2})$$

Therefore,

$$\dot{x_2} = \frac{x_1}{C} - \frac{x_2}{RC} \tag{A.1.2}$$

From Equation A.1.1,

$$\dot{x_1} = \frac{V_d P_o}{L} - \frac{r_L x_1}{L} - \frac{x_2}{L} \tag{A.1.3}$$

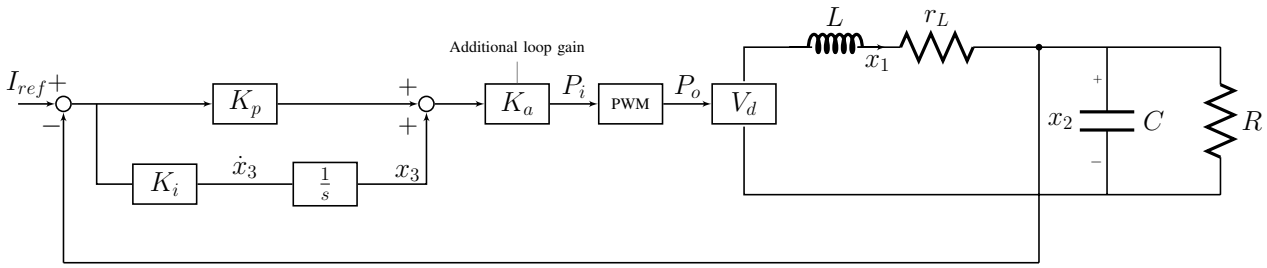

Figure A.1: Single current loop controller connected to buck converter

And

$$x_1 = c\dot{x_2} + \frac{x_2}{R} \tag{A.1.4}$$

From analysing the circuit, $i = x_1$ therefore,

$$\begin{aligned} \dot{x_3} &= K_i(I_{ref} - i) \\ &= K_i(I_{ref} - x_1) \end{aligned} \tag{A.1.5}$$

The state space representation $\mathbf{Ax}+\mathbf{B}$ of the single current loop controller derived using the above equations is is shown below:

$$\begin{bmatrix} \dot{x_1} \\ \dot{x_2} \\ \dot{x_3} \end{bmatrix} = \begin{bmatrix} \frac{-r_L}{L} & \frac{-1}{L} & 0 \\ \frac{-1}{C} & \frac{-1}{RC} & 0 \\ \frac{-K_i}{l} & 0 & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} + \begin{bmatrix} \frac{V_d P_o}{L} \\ 0 \\ K_i I_{ref} \end{bmatrix}$$

The $\mathbf{C}$ matrix is determined as:

$$i = \begin{bmatrix} 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix}$$

There are two $\mathbf{B}$ matrices depending on the output of the modulator, shown below:

$$B_1 = \begin{bmatrix} \frac{V_d}{L} \\ 0 \\ K_i I_{ref} \end{bmatrix}$$

and

$$B_2 = \begin{bmatrix} 0 \\ 0 \\ K_i I_{ref} \end{bmatrix}$$

The output P_i of the modulator is calculated as:

$$\begin{aligned} P_i &= K_p(I_{ref} - i) + x_3 \\ &= K_p(I_{ref} - \mathbf{C}x) + x_3 \end{aligned} \tag{A.1.6}$$

The particular solution of the two switching states are: State 1 when $(P_o = 1)$

$$x_{p1} = \begin{bmatrix} \frac{V_d}{r_L + R} \\ \frac{V_d R}{R + r_L} \\ K_i(I_{ref} - \frac{V_d}{r_L + R})t \end{bmatrix}$$

and State 2 when$(P_o = 0)$

$$x_{p2} = \begin{bmatrix} 0 \\ 0 \\ K_i I_{ref} \end{bmatrix}$$

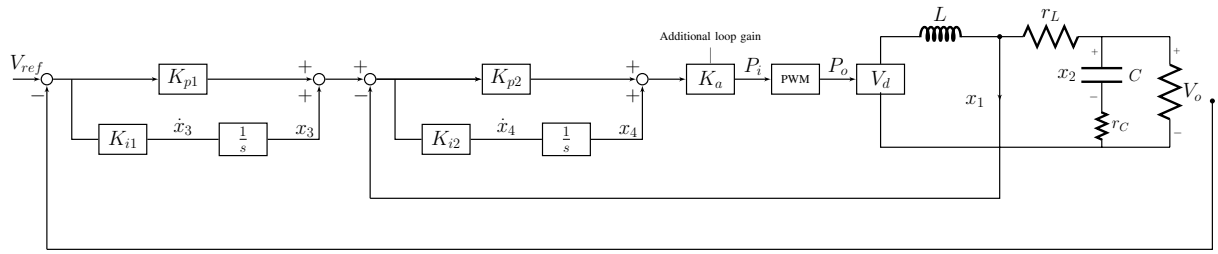

Figure A.2: Dual loop voltage and current controller connected to buck converter

A.2 Derivation of the state-space representation of the dual loop voltage and current controller

From analysing the circuit the following equations are obtained.

$$V_d Po = L\dot{x_1} + R_L x_1 x_2 + r_c C\dot{x_2} \tag{A.2.1}$$

and,

$$x_2 + r_C C\dot{x_2} = R(x_1 - C\dot{x_2}) \tag{A.2.2}$$

Moreover,

$$\dot{x_2} C(R + r_C) = Rx_1 - x_2 \tag{A.2.3}$$

Therefore,

$$\dot{x_2} = \frac{R}{C(R + r_C)} x_1 - \frac{1}{C(R + r_C)} x_2 \tag{A.2.4}$$

By substituting for Equation A.2.1,

$$V_d P_o = Lx_1 + r_L x_1 + x_2 + \frac{r_C R}{R + r_C} x_1 - \frac{r_C}{R + r_c} x_2 \tag{A.2.5}$$

Therefore,

$$\dot{x_1} = \frac{1}{L}\left(\frac{Rr_L + r_C r_L + r_C R}{R + r_C}\right) x_1 + \frac{-1}{L}\left(\frac{R}{R + r_L}\right) x_2 + \frac{V_d P_o}{L} \tag{A.2.6}$$

The output voltage is calculated as:

$$\begin{aligned} V_o &= R(x_1 - C\dot{x_2}) \\ &= \frac{Rr_C}{R + r_C} x_1 + \frac{R}{R + r_C} x_2 \end{aligned} \tag{A.2.7}$$

The derivative $\dot{x_3}$ is determined as:

$$\begin{aligned} \dot{x_3} &= K_{i1}(V_{ref} - V_o) \\ &= k_{i1}\left(V_{ref} - \frac{Rr_c}{R + r_C} x_1 - \frac{R}{R + r_C}\right) \end{aligned} \tag{A.2.8}$$

Moreover,

$$\begin{aligned}\dot{x_4} &= K_{i2}\left(K_{p1}(V_{ref}-V_o)+x_3-x_1\right)\\ &= K_{i2}\left[K_{p1}\left(V_{ref}-\frac{Rr_C}{R+r_C}x_1-\frac{R}{R+r_C}x_2\right)+x_3-x_1\right]\\ &= -K_{i2}\left(1+\frac{K_{p1}Rr_C}{R+r_C}\right)x_1-\frac{K_{p1}K_{i2}R}{R+r_C}x_2+K_{i2}x_3+K_{p1}K_{i2}V_{ref}\end{aligned} \tag{A.2.9}$$

Using the equations derived above, the state space vector **A** is determined as:

$$A=\begin{bmatrix}\frac{-1}{L}\left(\frac{Rr_L+r_Cr_L+r_CR}{R+r_C}\right) & \frac{-1}{L}\left(\frac{R}{R+r_C}\right) & 0 & 0\\ \frac{R}{C(R+r_C)} & \frac{-1}{C(R+r_C)} & 0 & 0\\ \frac{-K_{i1}Rr_C}{R+r_C} & \frac{-RK_{i1}}{R+r_C} & 0 & 0\\ -K_{i2}(1+\frac{K_{p1}Rr_C}{R+r_C}) & \frac{-K_{i2}K_{p1}R}{R+r_C} & K_{i2} & 0\end{bmatrix}$$

The two **B** matrices depends on the output of the pulse width modulator. The **B** matrices are illustrated in the following equations:

$$B_1=\begin{bmatrix}\frac{V_d}{L}\\ 0\\ K_{i1}V_{ref}\\ K_{p1}K_{i2}V_{ref}\end{bmatrix}$$

and,

$$B_2=\begin{bmatrix}0\\ 0\\ K_{i1}V_{ref}\\ K_{p1}K_{i2}V_{ref}\end{bmatrix}$$

The **C** is represented by:

$$C=\begin{bmatrix}\frac{Rr_C}{R+r_C} & \frac{R}{R+r_C} & 0 & 0\end{bmatrix}$$

The output P_i of the inner loop PI controller is determined as:

$$P_i = K_{p2}\left((K_{p1}(V_{ref}-V_o)+x_3)-x_1\right)+x_4 \tag{A.2.10}$$

The particular solutions for State 1 when $P_o = 1$) and State 2 when $P_o = 0$) are shown in the following equations:

$$x_{p1}=\begin{bmatrix}\frac{V_d}{r_L+R}\\ \frac{RV_d}{R+r_L}\\ K_{i1}(V_{ref}-\frac{V_dR}{R+r_L})t\\ K_{i2}t\left[K_{i1}(V_{ref}-\frac{V_dR}{R+r_L})t+K_{pi}(V_{ref}-\frac{V_dR}{R+r_L})\right]\end{bmatrix}$$

and

$$x_{p2} = \begin{bmatrix} 0 \\ 0 \\ K_{i1}V_{ref}t \\ K_{i2}t(K_{i1}V_{ref}t + K_{p1}V_{ref}) \end{bmatrix}$$

Appendix B

PCB Schematics and Layouts

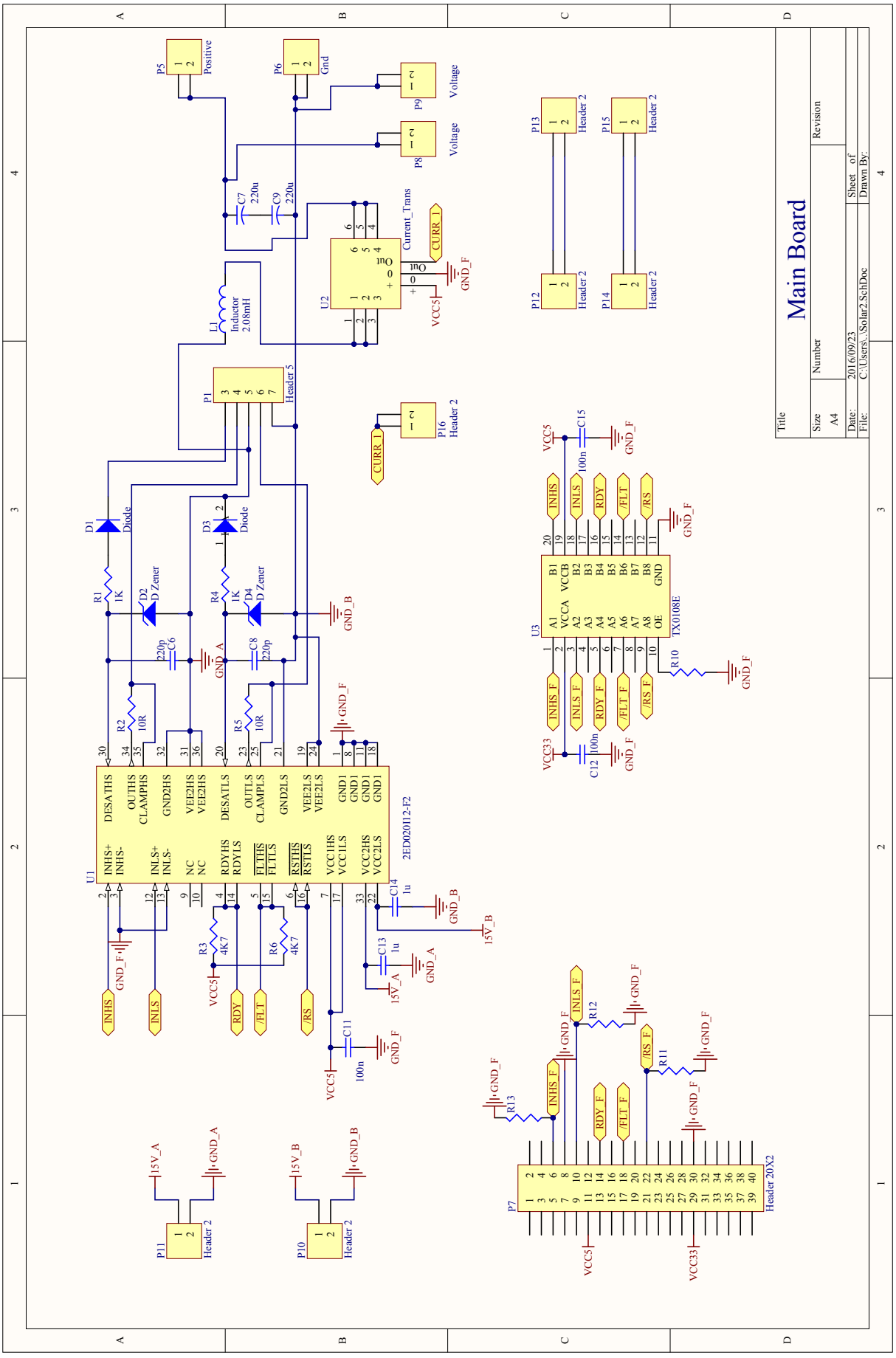

Figure B.1: Synchronous buck converter main circuit

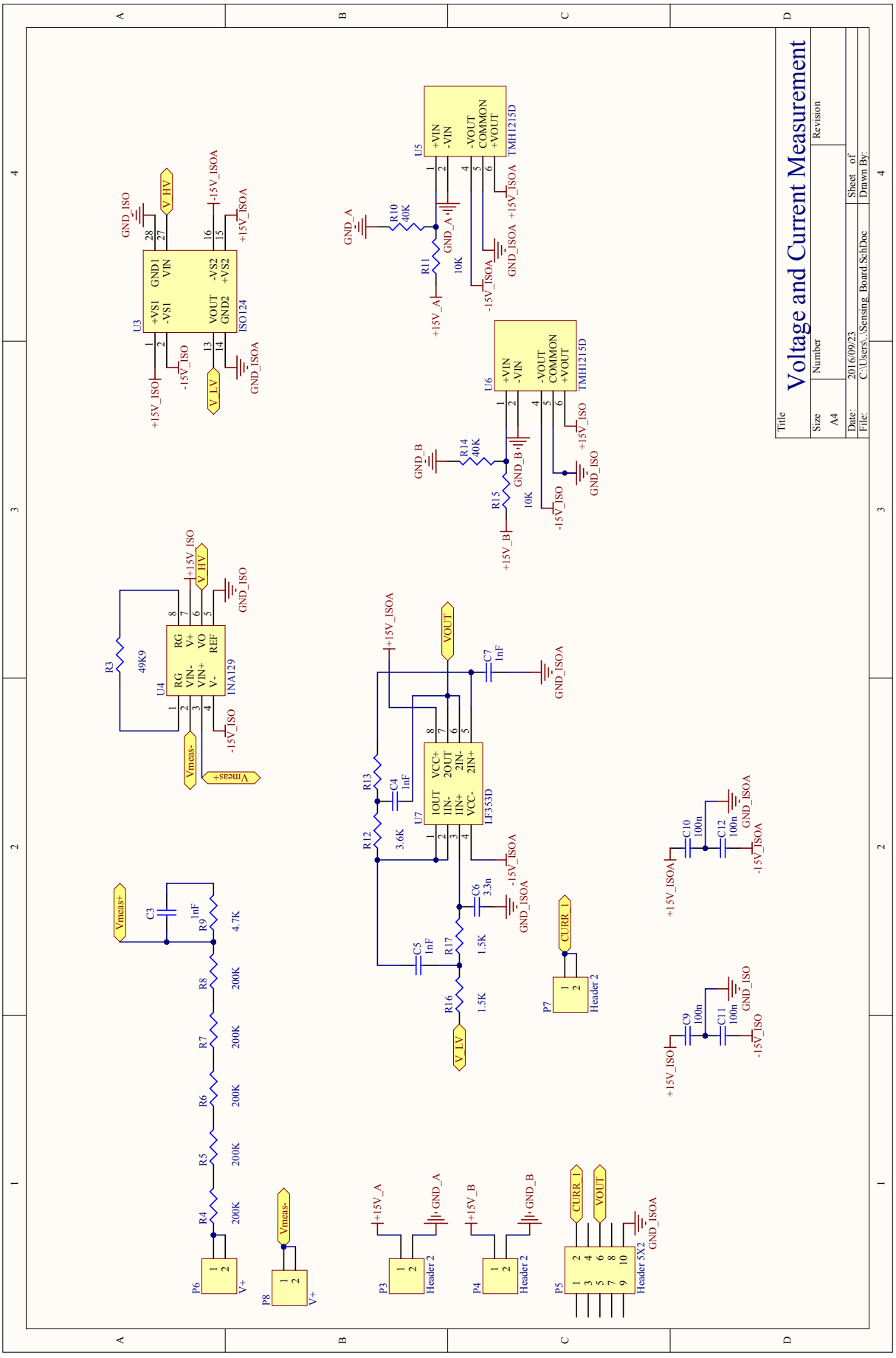

Figure B.2: Voltage and current measurement circuit

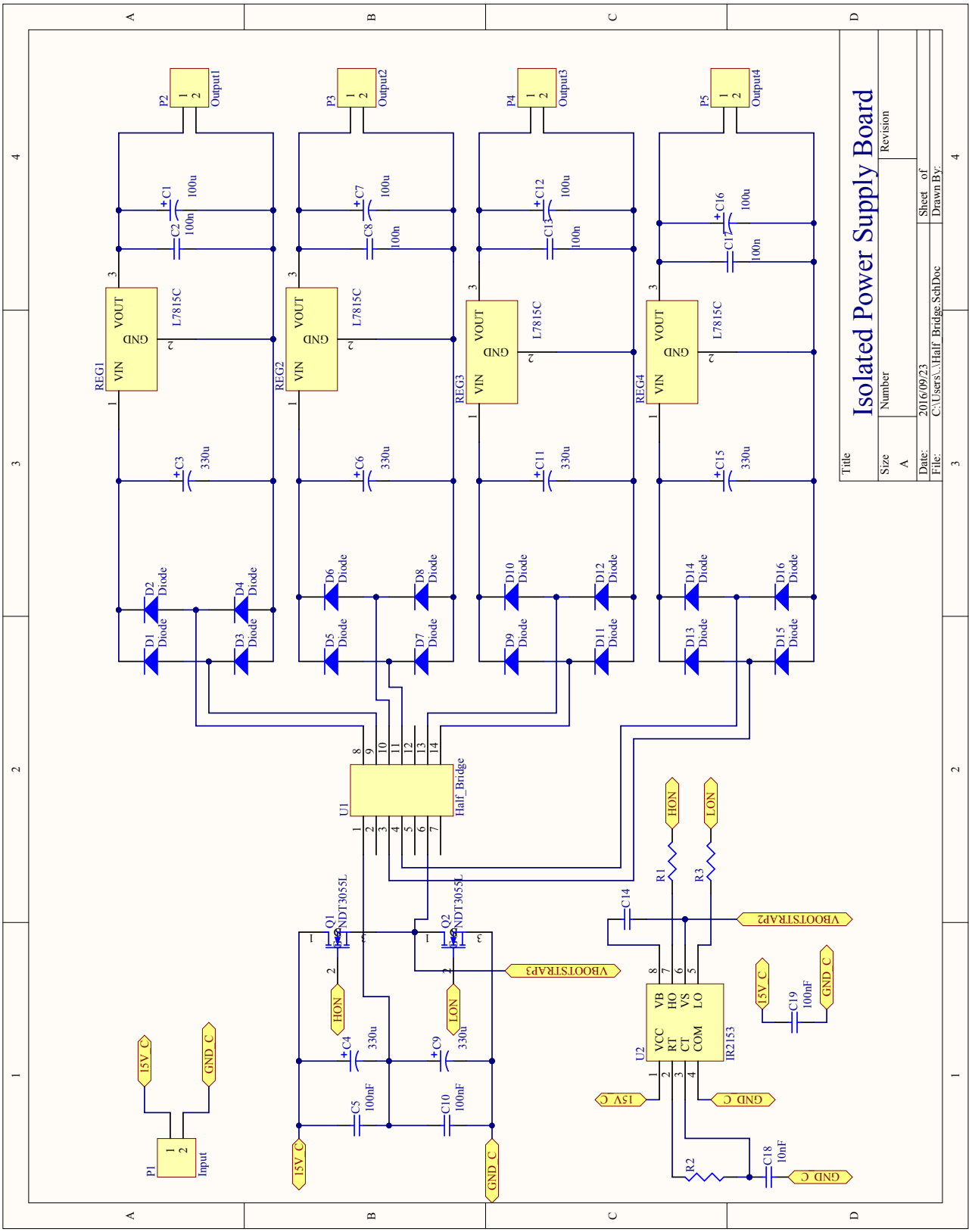

Figure B.3: Isolated power supply circuit

Appendix C

Synchronous Buck converter

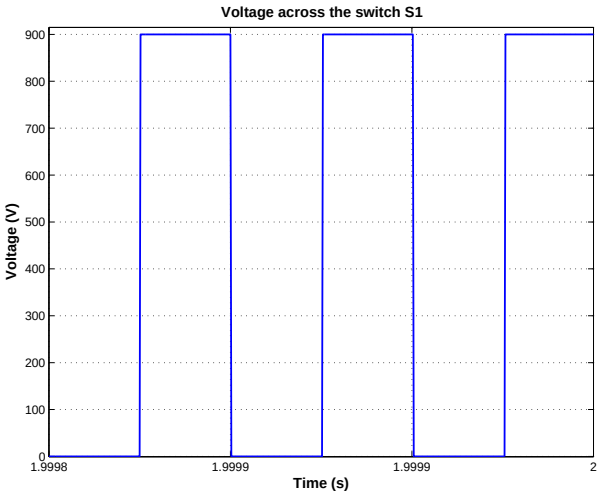

Figure C.1: Simulated voltage V_{s1}

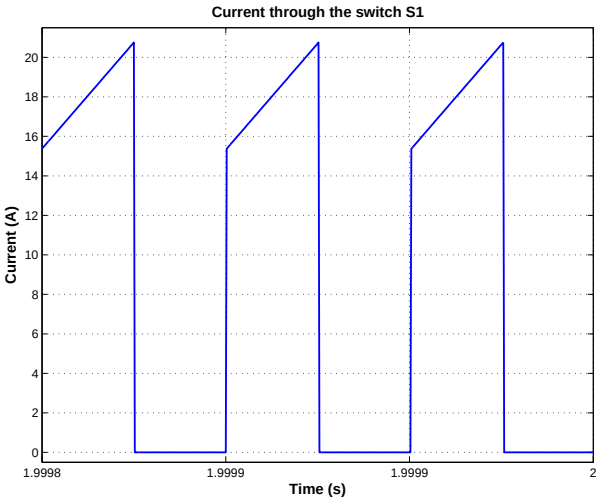

Figure C.2: Simulated current i_{s1}

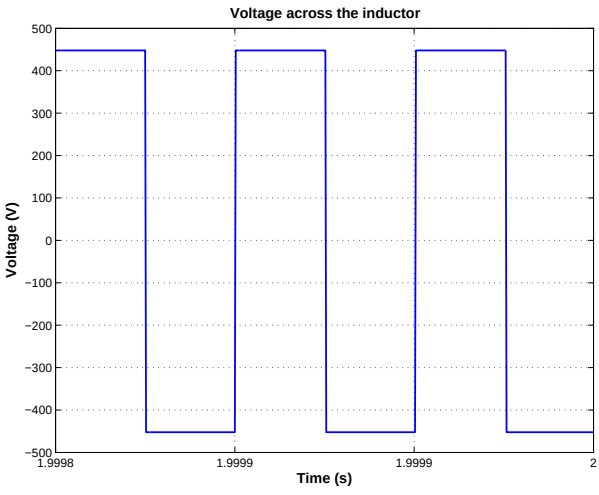

Figure C.3: Simulated voltage V_L

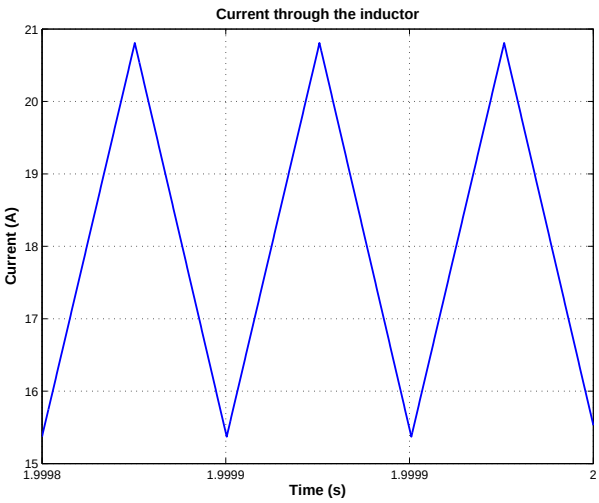

Figure C.4: Simulated current i_L

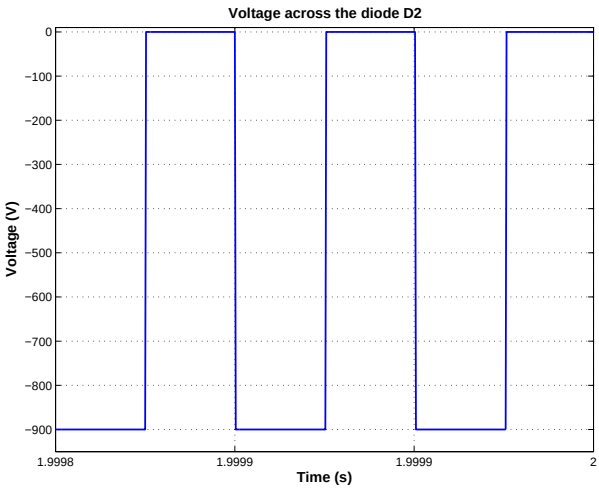

Figure C.5: Simulated voltage V_{D2}

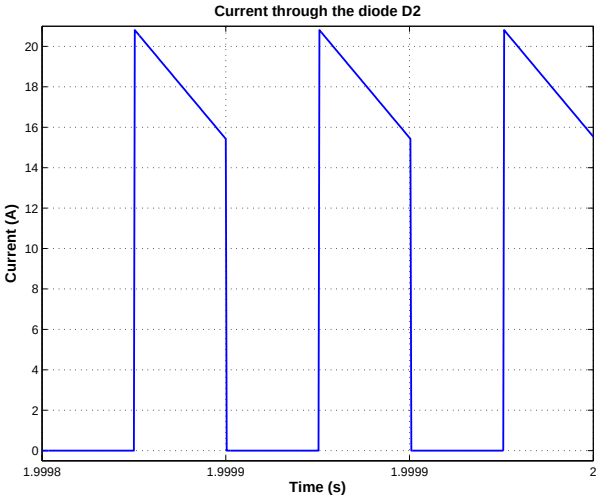

Figure C.6: Simulated current i_{D2}

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